

SONY®

APR-5000
TECHNICAL SERVICE
TRAINING MANUAL

Prepared by:
SONY PROFESSIONAL AUDIO TRAINING GROUP

**APR-5000 TRAINING MANUAL
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SECTION 1 INTRODUCTION

1.0 Overview

The APR-5000 Series represents a line of full-feature professional audio recorder/reproducers for broadcasting, recording studio, video, and film production environments. This machine incorporates the latest digital technology available, with computer controlled transport and audio electronic techniques unsurpassed by any other recorder of its type.

The transport is built around a high-strength, low-mass aluminum casting, and is mechanically designed so that all boards are easily accessible. A 16-bit microprocessor corrects for any variations in transport operation, offering precise speed stability and superior tape handling.

The servo controlled capstan motor is referenced by the microprocessor controller to a quartz crystal, and is built with a ceramic shaft for durability and accurate operation.

Tedious trim pot audio adjustments have been replaced with a microprocessor-controlled alignment feature. Up to three separate alignments can be stored per speed, allowing for maximum flexibility when changing between alternative tape types, reference fluxivities, overbias settings, or record/reproduce equalization standards. This allows the calibration of the machine to be changed at the push of a button. Also, each headstack has its own identification code, making it possible to store another complete set of preset alignments for each different headstack type.

Both serial and parallel remote control ports are provided for integration with external automation and editing systems. Remote and local synchronization features are available for EBU, SMPTE Drop Frame, and SMPTE Non-Drop Frame Time Code formats, as well as for VITC and pilot tone signals.

The APR-5000 establishes a new level of functional intelligence and overall flexibility in an analog professional recorder. It is available in desktop and console configurations for ease of installation in any environment.

1.1 Standard Models

The APR-5000 Series is available in four standard versions:

APR-5001

Mono version. It uses 1/4-inch tape, recording in the full-track format, and is available as a high speed or a low speed unit.

APR-5002

Two-track version. This is available in 1/4-inch and 1/2-inch models. The 1/4-inch unit comes in high or low speeds, with NAB, DIN, or NAB Amorphous heads.

APR-5003

Time code, center track version, It is available in 1/4-inch and high speed models only.

APR-5003V

Vertical Interval Time Code version. Contains all the features found in the APR-5003, along with provisions for Resolve on Play and synchronization to external VITC and pilot tones.

1.2 Options

The following is a description of the optional accessories available for the APR-5000 Series.

SU-14 Stand

This variable profile stand converts the APR-5000 from a desk top to a stand-alone model.

RM-5010 Remote Control Unit

This unit allows for control of the transport and recording functions of the APR-5000 from a remote location.

APR-5010 Editing Scissors

A useful tool in any editing environment, the Editing Scissors cut the tape directly at the APR-5000 headstack, thus expediting the production process. Factory installation is required.

MB-5000 Side Brackets

These brackets effectively extend the working space available on the top of the APR-5000 deck, and are useful as an editing table, producers desk, etc.

1.3 Specifications

All specifications are typical at 25 degrees C, and are subject to change without notice. Sony reserves the right to make alterations in features and specifications as technical progress may warrant.

Weight	91 pounds (46.26 Kg.)
Weight (With SU-14 Stand Option)	138 pounds (70.15 Kg.)
Normal Operating Temperature Range	+41 F to +95 F (+5 C to +35 C)
Storage Temperature	-4 F to +158 F (-20 C to 70 C)
Specification Guarantee Temperature	+77 F (+25 C)
Humidity	10 to 90 (Non-condensing)
Operating Position (With SU-14 Stand Option)	Horizontal or 15 tilt

Table 1-1. Mechanical Specifications

POWER REQUIREMENTS	Selectable AC Volts at 48 to 64Hz: 100/110/120/200/220/240
POWER CONSUMPTION	300 Watts Maximum
FUSE RATING	5A(100V), 4A(110), 2A(200V) Normal Load Fuse
REEL SIZE (metal or plastic)	3 to 12.5 inches, NAB or EIA (DIN hubs optional)
TAPE TENSION NOMINAL	120 grams
TAPE SPEED	Standard high speed: 7.5, 15, and 30ips Low speed models: 3.75, 7.5, and 15 ips Variable speed: +/- 50% of fixed speed
SPEED STABILITY	Better than 0.02%
FAST WIND TIME	110 sec for 2400 feet of tape 170 sec for 4800 feet of tape
SPOOL WIND TIME	370 sec for 2400 feet of tape
MVC VELOCITY	From full stop to 1.9 meters per second, in either direction
flutter START UP TIME/ FLUTTER SPECIFICATION w/ 10.5-inch reels	%DIN 45507 900 msec at 30 ips 0.3% 500 msec at 15 ips 0.15% 500 msec at 15 ips 0.15%

Table 1-2. Transport Specifications

1=CLOSED
 0=OPEN

Headstack ON
 Low 3.75-15 ips
 High 7.5-30 ips

$\frac{1}{4}$ " A	$\frac{1}{4}$ " A	$\frac{1}{4}$ " A
$\frac{1}{4}$ " B	$\frac{1}{4}$ " B	$\frac{1}{4}$ " B
-	$\frac{1}{4}$ " C	$\frac{1}{2}$ " A
-	$\frac{1}{4}$ " D	$\frac{1}{2}$ " B
-	$\frac{1}{2}$ " A	-
-	$\frac{1}{2}$ " B	-

Mono
 2 TK
 3 TK

1 2 3 4 5 6 7 8							
-----OPEN-----							
1							
	0 1						
		0 0 0 1 1 1	0 1 1 0 0 1	1 0 1 0 1 0			
				0 0 0	0 1 1	1 0 1	

In the $\frac{1}{4}$ " format:

A is assigned to NAB heads
 B is assigned to Amorphous heads
 C is assigned to DIN heads

In the $\frac{1}{2}$ " format:

A is assigned to NAB heads

Figure 1-3. Headstack ID DIP Switch Setting

AUDIO AMPLIFIER ELECTRONICS	Input Impedance 10k ohms Output Impedance 120 ohms Output Clipping +24dBm (no load condition)								
BIAS FREQ	400kHz								
ERASE FREQ	100kHz								
WOW AND FLUTTER (DIN 45507 weighted)	Less than 0.025% at 30 ips Less than 0.035% at 15 ips Less than 0.055% at 7.5 ips Less than 0.100% at 3.75 ips								
DISTORTION 30 ips AES 15 ips NAB 7.5 ips NAB 3% third harmonic fluxivity level	Harmonic distortion referenced to a level of 510nWb/m 1kHz fundamental frequency: <table border="0" style="width: 100%;"> <tr> <td style="width: 50%; vertical-align: top;"> 3rd Harmonic Less than 0.35% Less than 0.52% Less than 1.60% </td> <td style="width: 50%; vertical-align: top;"> 2nd Harmonic Less than 0.10% ; Less than 0.10% ; Less than 0.10 ; </td> </tr> </table> <table border="0" style="width: 100%; margin-top: 10px;"> <tr> <td style="width: 50%;">30 ips AES</td> <td style="width: 50%;">1040nW/b</td> </tr> <tr> <td>15 ips NAB</td> <td>1020nW/b</td> </tr> <tr> <td>7.5 ips NAB</td> <td>1000nW/b</td> </tr> </table>	3rd Harmonic Less than 0.35% Less than 0.52% Less than 1.60%	2nd Harmonic Less than 0.10% ; Less than 0.10% ; Less than 0.10 ;	30 ips AES	1040nW/b	15 ips NAB	1020nW/b	7.5 ips NAB	1000nW/b
3rd Harmonic Less than 0.35% Less than 0.52% Less than 1.60%	2nd Harmonic Less than 0.10% ; Less than 0.10% ; Less than 0.10 ;								
30 ips AES	1040nW/b								
15 ips NAB	1020nW/b								
7.5 ips NAB	1000nW/b								
DISTORTION/ NOISE SPECIFICATION DISCLAIMER	Distortion and record/reproduce noise are primarily functions of tape formulation and may vary from one formulation to another, even from one reel of tape to another. Bias settings play a very significant role in the case of distortion, and are a user-chosen parameter based on average program fluxivity and desired frequency response. The specifications shown indicate achievable performance with 3M Scotch 226 at reference fluxivity of 250nW/b for the standard NAB head configuration.								

Table 1-3. Audio Specifications

FREQUENCY RESPONSE									
Speed	Record/Repro				Record/Sync				
30ips AES	50Hz to 28kHz,+.75/-3dB				50Hz to 20kHz,+.75/-3dB				
15ips NAB	30Hz to 24kHz,+.75/-2dB				30Hz to 16kHz,+.75/-2dB				
7.5ips NAB	20Hz to 20kHz,+.75/-2dB				20Hz to 8kHz,+.75/-2dB				
SIGNAL TO NOISE, RECORD/REPRODUCE									
Speed	Unweighted (See note 2)				Weighted dB(A)				
30ips AES	-64dB				-68dB				
15ips NAB	-62dB				-64dB				
7.5ips NAB	-61dB				-64dB				
DEPTH OF ERASE, 1KHZ TONE	ERASE/BIAS CROSSTALK TO AUDIO								
	Better than -76dB at 30 ips								
	Less than 150mVpp at 7.5 ips								
GAP COMPENSATIONS									
Speed	RGC	SGC	RCF	RCB					
30 ips	C1	C1	C0	C1					
15 ips	CA	CC	C9	C5					
7.5 ips	CB	CE	C4	C3					
HEADSTACK DIP SWITCH SETTINGS									
	DIP switch	1	2	3	4	5	6	7	8
	Code setting	1	1	0	0	1	0	0	1
NOTES:	<p>1. Unless otherwise noted, all audio specifications are referenced to 250nW/m, using 3M Scotch 226.</p> <p>2. 20Hz to 20kHz third order harmonics.</p>								

Table 1-4. 1/4 inch Mono NAB Specifications

FREQUENCY RESPONSE									
Speed	Record/Repro	Record/Sync							
30ips AES	50Hz to 28kHz, +.75/-3dB	50Hz to 20kHz, +.75/-3dB							
15ips NAB	30Hz to 24kHz, +.75/-2dB	30Hz to 16kHz, +.75/-2dB							
7.5ips NAB	20Hz-20kHz, +.75/-1.5dB	20Hz to 8kHz, +.75/-2dB							
SIGNAL TO NOISE, RECORD/REPRODUCE									
Speed	Unweighted (See note 2)	Weighted dB(A)							
30ips AES	-59dB	-64dB							
15ips NAB	-56dB	-61dB							
7.5ips NAB	-56dB	-61dB							
DEPTH OF ERASE, 1KHZ TONE	ERASE/BIAS CROSSTALK TO AUDIO Better than -76dB at 30 ips Less than 150mVpp at 7.5 ips								
GAP COMPENSATIONS									
Speed	RGC	SGC	RCF	RCB					
30 ips	C1	C1	C0	C1					
15 ips	CA	CC	C9	C5					
7.5 ips	CB	CE	C3	C3					
HEADSTACK DIP SWITCH SETTINGS									
	DIP switch	1	2	3	4	5	6	7	8
	Code setting	1	1	0	0	1	0	1	0
NOTES:	1. Unless otherwise noted, all audio specifications are referenced to 250nW/m, using 3M Scotch 226. 2. 20Hz to 20kHz third order harmonics.								

Table 1-5. 1/4-inch 2-Track NAB Specifications

FREQUENCY RESPONSE									
Speed	Record/Repro				Record/Sync				
30ips AES	50Hz to 28kHz,+.75/-3dB				50Hz to 20kHz,+.75/-3dB				
15ips IEC	30Hz to 24kHz,+.75/-2dB				30Hz to 16kHz,+.75/-2dB				
7.5ips IEC	20Hz to 20kHz,+.75/-2dB				20Hz to 8kHz,+.75/-2dB				
SIGNAL TO NOISE, RECORD/REPRODUCE									
Speed	Unweighted (See note 2)				Weighted dB(A)				
30ips AES	-59dB				-64dB				
15ips IEC	-56dB				-61dB				
7.5ips IEC	-56dB				-61dB				
DEPTH OF ERASE, 1KHZ TONE	ERASE/BIAS CROSSTALK TO AUDIO								
	Better than -74dB at 30 ips Less than 150mVpp at 7.5 ips								
GAP COMPENSATIONS									
Speed	RGC	SGC	RCF	RCB					
30 ips	C1	C1	C0	C1					
15 ips	CA	CA	C3	C2					
7.5 ips	C4	C6	C4	C3					
HEADSTACK DIP SWITCH SETTINGS									
	DIP switch	1	2	3	4	5	6	7	8
	Code setting	1	1	0	1	1	0	1	0
NOTES:	<p>1. Unless otherwise noted, all audio specifications are referenced to 250nW/m, using 3M Scotch 226.</p> <p>2. 20Hz to 20kHz third order harmonics.</p>								

Table 1-6. 1/4 inch 2-Track DIN Specifications

NOTES:
continued

3. 7.5ips specifications are referenced to
79nWb/m, -10dB.

4. Ensure that all speeds are set to IEC
standard on the ALN Panel.

Table 1-6. 1/4 inch 2-Track DIN Specifications (continued)

FREQUENCY RESPONSE									
Speed	Record/Repro	Record/Sync							
30ips AES	35Hz to 25kHz,+.75/-3dB	37Hz to 25kHz,+.75/-3dB							
15ips NAB	22Hz to 24kHz,+.75/-2dB	25Hz to 20kHz,+.75/-2dB							
7.5ips NAB	15Hz to 22kHz,+.75/-2dB	18Hz to 10kHz,+.75/-2dB							
SIGNAL TO NOISE, RECORD/REPRODUCE									
Speed	Unweighted (See note 2)	Weighted dB(A)							
30ips AES	-62dB	-65dB							
15ips NAB	-57dB	-60dB							
7.5ips NAB	-56dB	-60dB							
DEPTH OF ERASE, 1KHZ TONE	ERASE/BIAS CROSSTALK TO AUDIO								
	Better than -76dB at 30 ips Less than 150mVpp at 7.5 ips								
GAP COMPENSATIONS									
Speed	RGC	SGC	RCF	RCB					
30 ips	C0	C0	C0	C1					
15 ips	C9	CA	C0	C5					
7.5 ips	C3	C6	C2	C3					
HEADSTACK DIP SWITCH SETTINGS									
	DIP switch	1	2	3	4	5	6	7	8
	Code setting	1	1	0	1	0	0	1	0
NOTES:	<p>1. Unless otherwise noted, all audio specifications are referenced to 250nW/m, using 3M Scotch 226.</p> <p>2. 20Hz to 20kHz third order harmonics.</p>								

Table 1-7. 1/4 inch 2-Track Amorphous NAB Specifications

FREQUENCY RESPONSE									
Speed	Record/Repro	Record/Sync							
30ips AES	40Hz to 25kHz,+.75/-3dB	40Hz to 25kHz,+.75/-3dB							
15ips NAB	25Hz to 24kHz,+.75/-2dB	20Hz to 20kHz,+.75/-2dB							
7.5ips NAB	25Hz to 22kHz,+.75/-2dB	20Hz to 10kHz,+.75/-2dB							
SIGNAL TO NOISE, RECORD/REPRODUCE									
Speed	Unweighted (See note 2)	Weighted dB(A)							
30ips AES	-62dB	-66dB							
15ips NAB	-59dB	-64dB							
7.5ips NAB	-59dB	-64dB							
DEPTH OF ERASE, 1KHZ TONE	ERASE/BIAS CROSSTALK TO AUDIO Better than -72dB at 30 ips Less than 100mVpp at 7.5 ips								
GAP COMPENSATIONS									
Speed	RGC	SGC	RCF	RCB					
30 ips	C1	C1	C0	C0					
15 ips	C9	CA	C1	C6					
7.5 ips	CB	CE	C6	C3					
HEADSTACK DIP SWITCH SETTINGS									
	DIP switch	1	2	3	4	5	6	7	8
	Code setting	1	1	1	0	1	0	1	0
NOTES:	1. Unless otherwise noted, all audio specifications are referenced to 250nW/m, using 3M Scotch 226. 2. 20Hz to 20kHz third order harmonics.								

Table 1-8. 1/2-inch 2-Track NAB Specifications

TIME CODE CENTER TRACK WIDTH		Ø.36 millimeters							
NOMINAL TIME CODE RECORDING LEVEL		700nWb/m (see note 1)							
INPUT LEVELS, BALANCED/ UNBALANCED (see note 2)		<u>MINIMUM</u> Ø.6vpp differential				<u>MAXIMUM</u> 2Øvpp differential			
OUTPUT LEVELS, BALANCED/ UNBALANCED (see notes 3 & 4)		<u>NOMINAL</u> 4.Øvpp differential				<u>MAXIMUM</u> 7.5vpp differential			
RS-422 TYPE OUTPUT (see note 4)		<u>MAX "Ø" LEVEL</u> 4.Øvpp differential				<u>MIN "1" LEVEL</u> 6.Øvpp differential			
TIME CODE CROSSTALK		Less than 85db at 15ips							
GAP COMPEN- SATIONS (track 3 only)									
Speed		RGC	SGC	RCF	RCB				
3Ø ips		--	CØ	CØ	CØ				
15 ips		--	C3	CØ	CØ				
7.5 ips		--	C3	CØ	CØ				
TRACK 3 PRESETS									
Speed		Sync Low Frequency	Sync High Frequency	Rec High Frequency	Bias Level				
3Ø ips		FF	ØØ	FF	3Ø				
15 ips		FF	ØØ	FF	2Ø				
7.5 ips		FF	ØØ	FF	1Ø				
HEADSTACK DIP SWITCH SETTINGS									
DIP switch		1	2	3	4	5	6	7	8
Code setting		1	1	Ø	Ø	1	Ø	1	1

Table 1-9. Time Code Track Specifications

TIME CODE/ TAPE TACH RELATION- SHIP	16 tach pulses per frame, SMPTE 19.2 pulses per frame, EBU
NOTES:	<ol style="list-style-type: none"> 1. Equivalent to 250nWb/m measured RMS. 2. Balanced input common mode rejection 10vpp (10Hz to 100kHz) 3. Differential analog output with JU-1 and JU-3 installed on the CNX board. 4. No damage will result if any of the outputs are shorted to ground.

Table 1-9. Time Code Track Specifications (continued)

TIME CODE READING CHARACTERISTICS (see note 1)		
External/Internal time code		
MINIMUM GUARANTEED READING RANGE IN PLAY MODE	+/- 50% of nominal speed	
INTERPOLATED READING RANGE IN FWD OR REV MODES	Up to transport limit speed	
READABLE RANGE, LOWER LIMIT	0.05 times nominal speed	
READABLE RANGE, UPPER LIMIT	70.0 times nominal speed	
OUTPUT SIGNAL SELECTION		
CHASE MODE/ STOP MODE	Buffered input time code signal.	
NON- CHASE MODES	PLAY	Longitudinally corrected time code from tape.
	NON- PLAY	Wide bandwidth time code from tape.
RECORDING GENERATOR ACCURACY	+/- 0.005% SMPTE NDF, EBU	

Table 1-10. Time Code Specifications

SYNCHRONIZATION ACCURACY		Less than +/- 50usec @ nominal speed
WIND SPEED LIMIT VALUES (see note 3)		
SPEED		
30ips 15ips 7.5ips	275ips (normal maximum wind speed) 225ips 112ips	
NOTES:	<ol style="list-style-type: none"> 1. Specified performance assumes ideal time code integrity. 2. Interpolated reading range of external time code is performed by sync word detection, while internal interpolation range relies upon timer roller tachometer information. 3. Enabled in TC DISPLAY mode with an argument of 1 stored in Storage Location #36. 	

Table 1-10. Time Code Specifications (continued)

<u>VIDEO INPUT/OUTPUT CONNECTORS</u>
Two BNC-type connectors with switchable 75-ohm termination
<u>INPUT LEVEL</u>
<u>COMPOSITE SYNC OR VIDEO SETTING (see note 1)</u>
Input impedance, 10k-ohm
Video Standard RS-170A level (nominal)
Sinewave input, 0.4vpp minimum, 6.0vpp maximum
Squarewave input, 0.2vpp minimum, 6.0vpp maximum

Table 1-11. Video Port Specifications

LOGIC SETTING (see note 2)

**Input impedance, 100k-ohm
(accommodates CMOS or TTL logic families directly)**

Sinewave input, 3.0vpp minimum, 20vpp maximum

Squarewave input, 1.5vpp minimum, 20vpp maximum

NOTES:

- 1. Jumper JU-1 installed on the VVT board.**
- 2. Jumper JU-2 installed on the VVT board.**

Table 1-11. Video Port Specifications (continued)

SECTION 2 INSTALLATION

2.0 Overview

This section covers the information required to properly receive and install an APR-5000 Series tape machine. Use this information together with the information contained in Section 3 (INSTALLATION) of the APR-5000 Operation and Maintenance Manual.

2.1 Unpacking

Inspect the carton for exterior damage before opening. If any concealed damage is discovered, notify your freight agent at once, and request him to make an inspection. Use caution when unpacking the APR-5000 to avoid damage to the contents of any of the boxes. Save the carton and packing material should it become necessary to ship the equipment to another destination.

2.1.1 Inventory Check List

Ensure that the following parts are in the box:

- (1) APR-5000
- (1) AC Power Cord
- (1) European Power Cord
- (1) APR-5000 Manual
- (1) Extender Board
- (1) 10.5 inch Reel
- (1) 10.5 inch Reel of Tape
- (2) NAB Reel Hubs
- (2) Reel Platter Shims
- (3) Fuses (2A/200V, 4A/110V, 5A/100V)
- (1) Headstack Cover
- (1) Package User Labels (50 ct.)

2.2 Operational Environment

For best results, it is recommended that the APR-5000 be installed in an area where it will not be exposed to direct sunlight or any other heat source. The unit should be operated in a temperature range of 5 degrees C to 35 degrees C (41 degrees F to 95 degrees F).

Place the tape recorder where there is sufficient air circulation, to prevent internal heat build up. Do not block the ventilating holes on the cabinet or the rear panel. If the air is stagnant in the area where the unit will be placed, a ventilation fan is suggested.

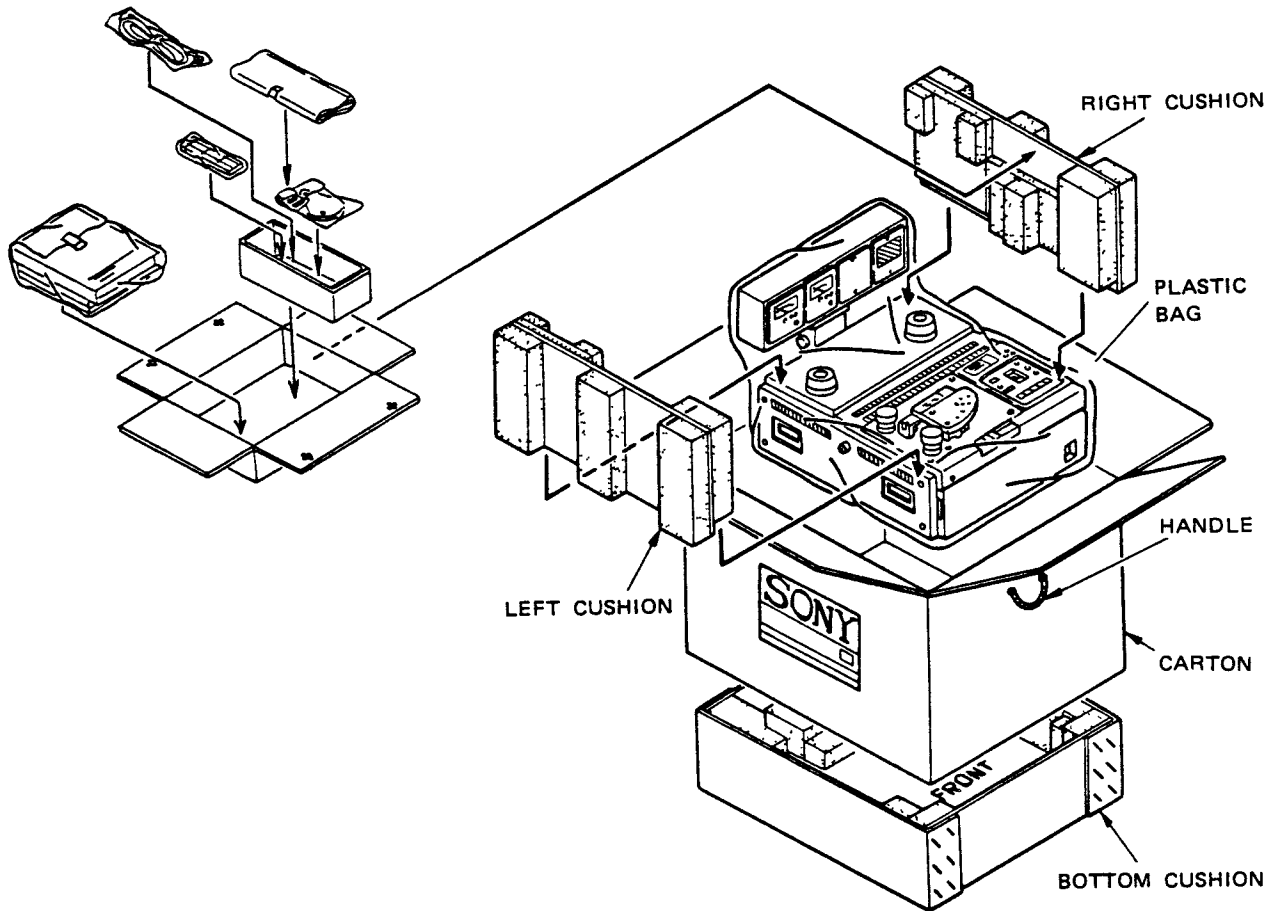


Figure 2-1. APR-5000 Packaging

2.3 Setting the Operating Voltage

The APR-5000 power line voltage can be set for any of six voltage levels, 100, 110, 120, 200, 220, or 240V. A warning sticker placed over the AC power connector on the tape recorder will inform the user of the voltage setting of the power supply when shipped from the factory.

Prior to connecting the AC power cord to the machine for the first time, make sure that the voltage selector is set to the appropriate position for the power service at your location. The following is a procedure for setting the power supply selector switches.

- STEP 1 Ensure that the AC power cord is disconnected from the machine.
- STEP 2 Remove the two retaining screws on the rear door, and open the door.
- STEP 3 Locate the two selector switches behind the take-up motor on the back of the power supply.
- STEP 4 Reset the switches to the appropriate voltage, as derived from Figure 2-2, if necessary.
- STEP 5 Close the rear door, and fasten with the two screws removed in Step 2.

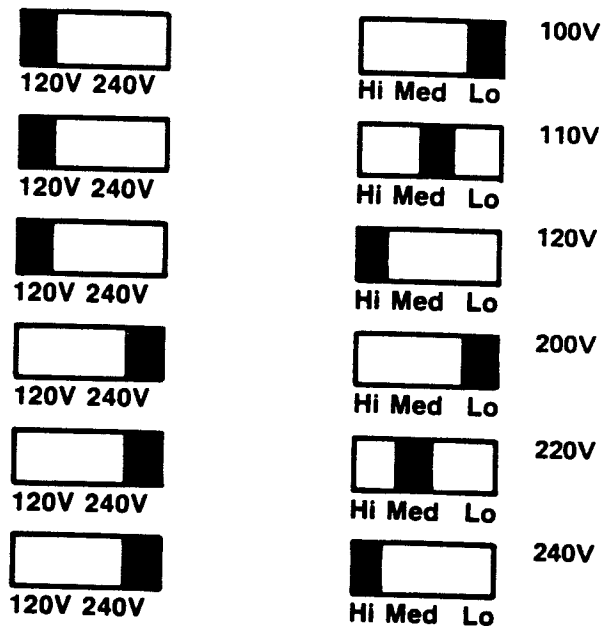


Figure 2-2. Power Supply Voltage Settings

2.4 SU-14 Stand Assembly

2.4.1 Supplied Parts

- (2) Vertical support members
- (2) Cross braces
- (1) Cover plate
- (8) 4x8 BZN screws
- (8) 4x8 PSW screws

2.4.2 Assembly Procedure

Refer to Figure 2-3 for this assembly procedure.

- STEP 1** Ensure that the three tapped screw holes on each vertical support member are facing forward, and that the tapped screw hole on each cross brace is facing forward as well. Then install the two cross braces to the two vertical support members using the eight 4x8 PSW screws.
- STEP 2** Using the eight 4x8 BZN screws, install the cover plate to the cross braces and to the vertical support members.
- STEP 3** Unscrew the hold down knobs so that the knob shafts do not protrude through the holes on either vertical support member.
- STEP 4** Remove the plastic cap from each vertical support member.
- STEP 5** Obtain assistance in order to lift the APR-5000 in STEP 6.
- STEP 6** Lift the APR-5000 using the side handles. Guide the machine into the stand assembly so that the slotted screw on each side panel of the tape machine fits into the slot atop each vertical support member. It may be necessary to adjust the slotted screws on the side panels so that they rest correctly in the slots.
- STEP 7** Carefully align the knob shafts into the desired hole on the side panel of the APR-5000 for either a horizontal or 15 degree mounting angle, and screw the hold down knobs finger-tight into place.
- STEP 8** Replace the plastic caps removed in STEP 4.

2.5 RM-5010 Remote Control Unit

The RM-5010 Remote Control Unit is the optional parallel remote control accessory for the APR-5000. It connects to the 50-pin parallel remote connector on the rear door, providing remote control and status control from up to 10 meters away.

The RM-5010 is easily connected to the APR-5000 by fastening the two screws on the Remote Control Unit connector end into the 50-pin receptacle on the rear door of the tape machine. Be sure to power off whenever connecting or disconnecting the RM-5010.

2.6 APR-5000 Series Cabinet Dimensions

Refer to the mechanical drawings shown in Figures 2-4, 2-5, and 2-6. All measurements are shown in millimeters. If it is required to convert these measurements into inches, use the formula:

$$n \text{ millimeters} \times .03937 = \text{equivalent inches}$$

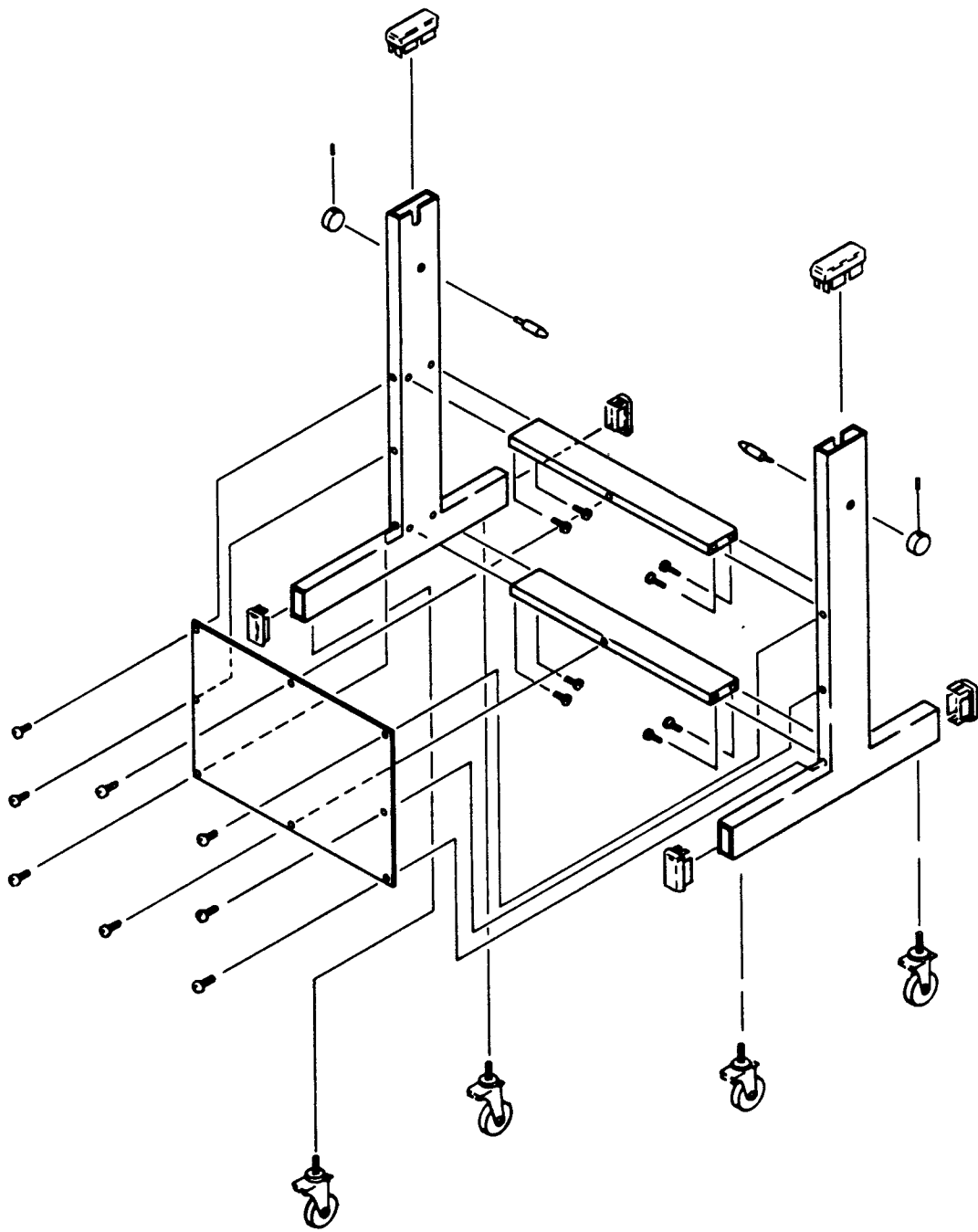


Figure 2-3. SU-14 Stand Assembly

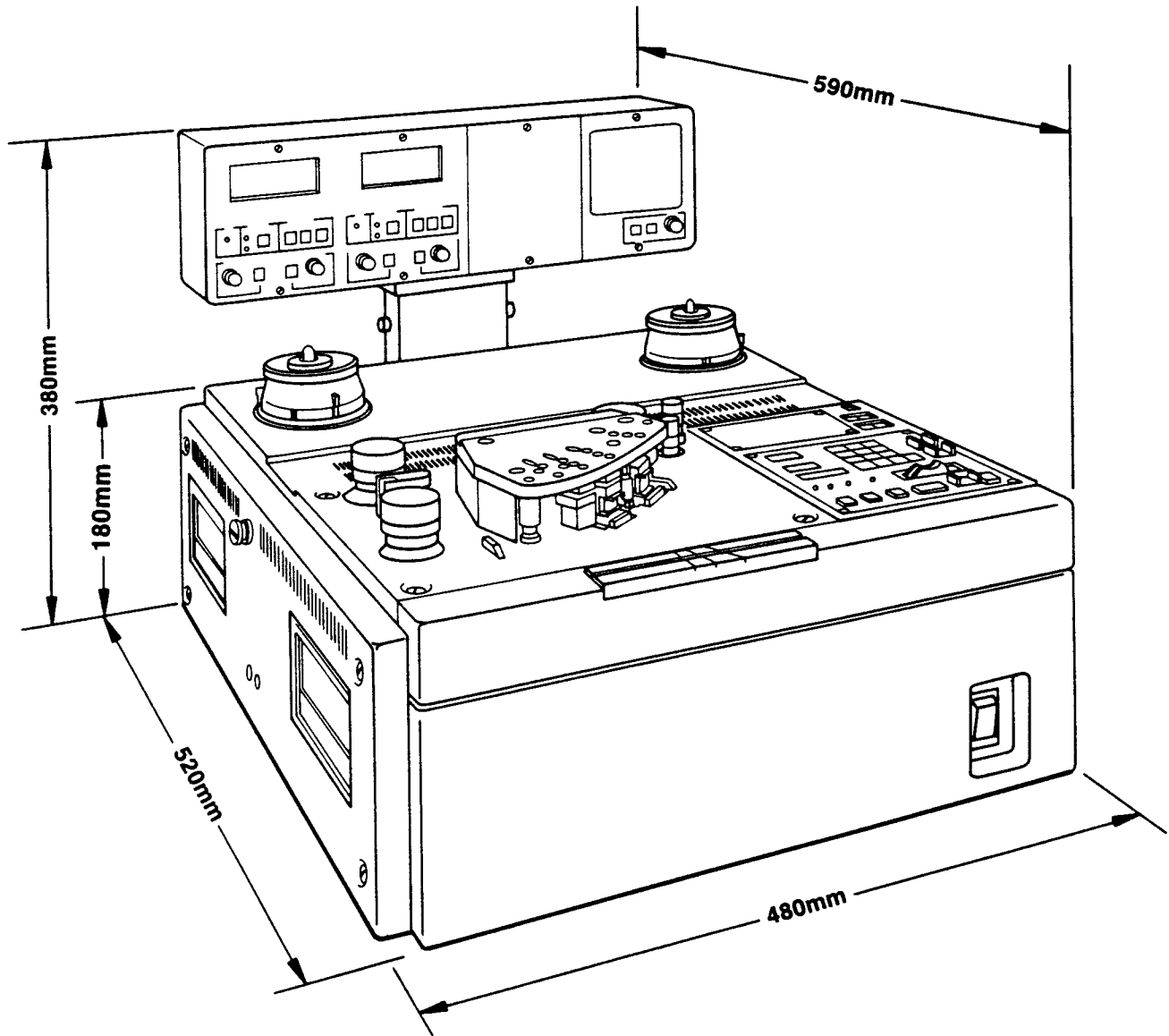


Figure 2-4. Overall Dimensions for APR-5000 Series (all)

(A) TABLE TYPE

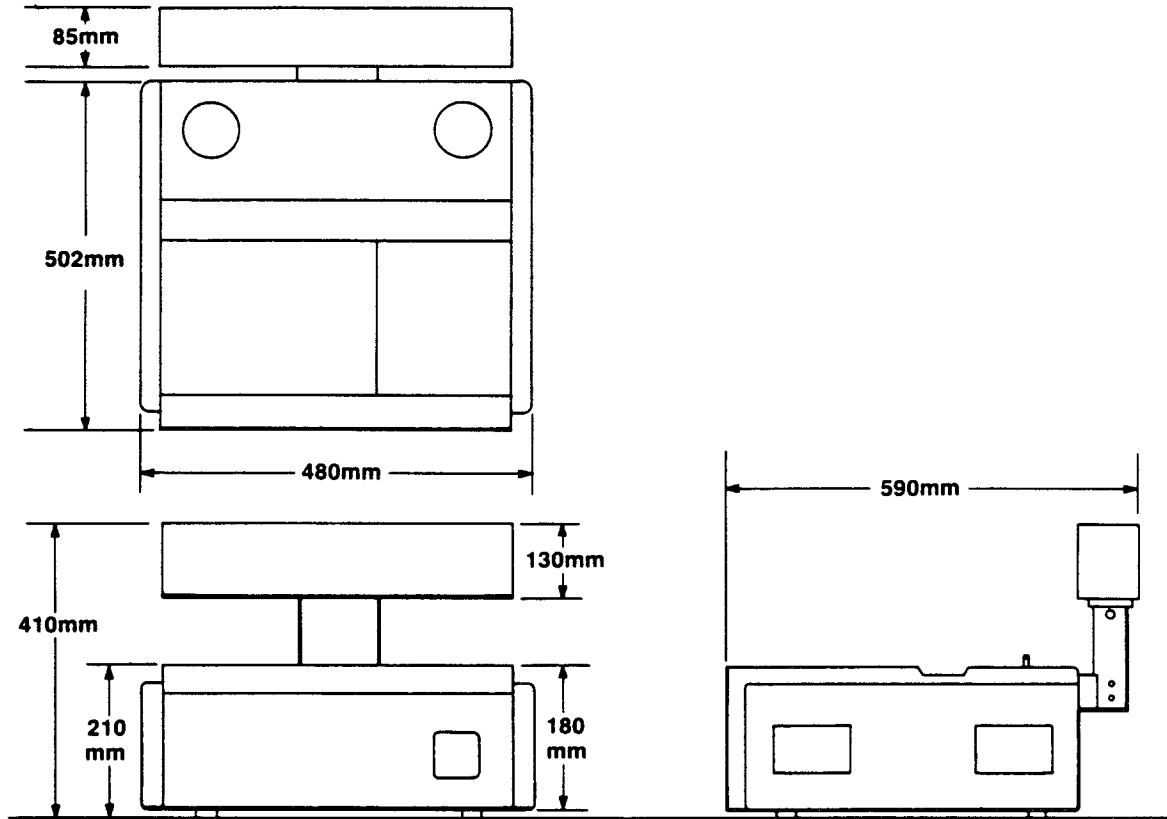


Figure 2-5. Overall Dimensions for APR-5000 Series (all)

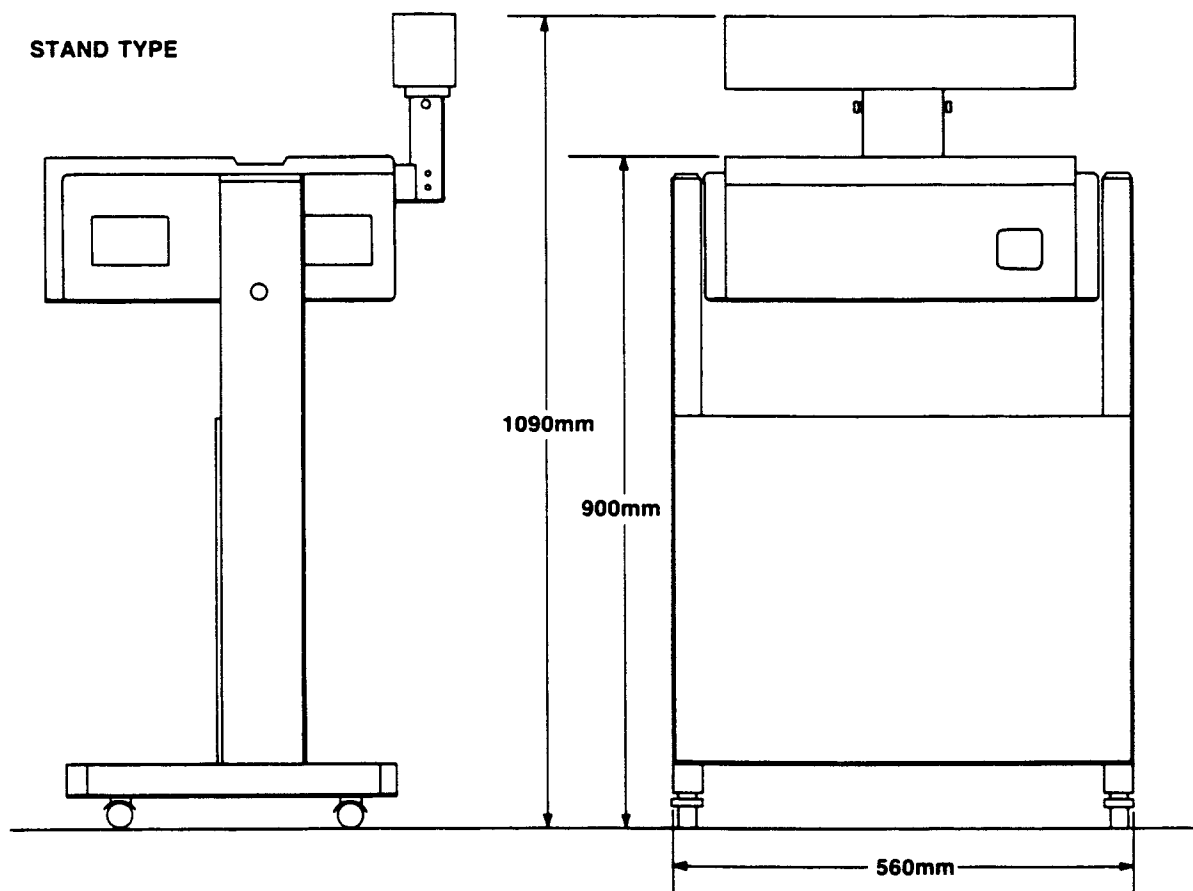


Figure 2-6. Overall Dimensions for APR-5000 Series (all)

2.7 Connection Example for the APR-5003V

The following diagram (Figure 2-7) illustrates the interconnection and set up of the APR-5003V recorder in a typical system. Refer to this drawing when installing or changing the system configuration.

Drawing missing in original

Figure 2-7. APR-5003V Interconnection

**SECTION 3
CONTROLS, INDICATORS
AND
OPERATIONAL GUIDELINES**

3.0 Overview

This section describes the transport, audio, Time Code, and editing operations of the APR-5000, so that the user may become familiar with all of the sophisticated operations that the machine is capable of performing. The status of the various machine controls and indicators upon initial power up is also provided. Use the information contained in this section in conjunction with the controls and indicators information found in the APR-5000 Operation and Maintenance Manual.

It should be noted that some of the functions described in this section may not be available on earlier software versions.

3.1 Initial Power Up

Once the machine has been properly installed as described in Section 2, power may then be applied. This section describes the various items related to the initial powering up of the machine.

3.1.1 Headstack ID DIP Switch

In order for the APR-5000 to operate properly, the Headstack ID DIP switch, must be set as shown in Figure 3-1. For more information on APR-5000 Headstack ID settings, refer to the appropriate specification chart in Section 1 of this manual.

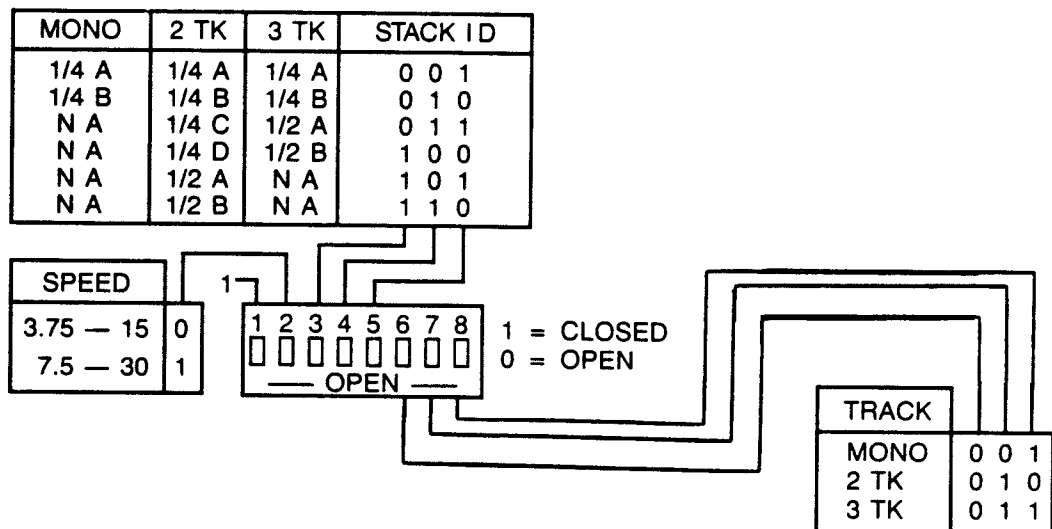


Figure 3-1. Settings for Headstack ID DIP Switch

3.1.2 Error Codes

When powered up, the machine goes through an internal CPU diagnostic sequence. If an error is detected, one of four Error Codes will be displayed in the STATUS Display on the Alignment (ALN) Panel. The STOP key will also flash to indicate that there is a failure.

The Error Codes are defined as follows:

HE (Headstack Error)

This indicates that the headstack identification code DIP switch is set improperly. If this error occurs, turn the power to the unit OFF and remove the headstack. Ensure that the DIP switch setting is valid (refer to the specifications charts in Section 1 of this manual). Replace the headstack onto the machine and proceed.

HI (Headstack Invalid)

This indicates that the headstack identification code DIP switch setting is invalid for the machine (i.e. 4-Track, 8-Track, etc.). If this error occurs, turn the power to the unit OFF and remove the headstack. Ensure that the DIP switch setting is valid (refer to the specifications charts in Section 1 of this manual). Replace the headstack onto the machine and proceed.

HO (Headstack Off)

This error indicates that the headstack connector is probably not mated correctly. The Headstack Poll signal (sent from the CPU board) is not returning to the CPU from the headstack assembly. To correct this problem, check the connection on the headstack mating connector and ensure proper contact.

PE (Preset Error)

This indicates that the alignment conditions stored in this preset are invalid. This condition will exist when the Lithium battery on the CPU board has been replaced. To alleviate this condition, perform a complete audio system alignment as described in Section 6.6 of this manual. Remember that, when aligning the machine as a result of this error, it is required to align the secondary functions as well. The secondary functions are:

RGC : Repro head Gap Compensation
SGC : Sync head Gap Compensation
RCF : ReCord feed-Forward Compensation
RCB : ReCord feed-Back Compensation

3.1.3 Controls and Indicators Status

Once the APR-5000 passes the internal diagnostic tests, the status of the various controls and indicators should be as follows:

Local Control Panel

NETWORK key indicator - illuminated;
LOCAL key indicator - illuminated;
TAPE SPEED - previous power down state;
STOP key indicator - illuminated;
TAPE TIME Display - 00:00:00:0. (00:00:00:00 in TC mode)

NOTES:

- The APR-5003V software is set to provide the user with information pertaining to the validity of the signals to be synchronized, as well as reel radius. The TAPE TIME Display on the Local Control Panel is used to display the following data.

Hours Decimal Point = Valid Video Reference Signal
Minutes Decimal Point = Valid Master Time Code
Seconds Decimal Point = Valid Slave Time Code
Frames Decimal Point = Valid Radius Not Established *

- The Frames (F) decimal point in the TAPE TIME Display is used to monitor the establishment of a valid radius condition. When illuminated, the decimal point indicates that the machine does not have a valid radius reference. Loading a reel of tape usually establishes a valid reference, but sometimes it is necessary to manually move the tape seven and one half inches to extinguish the decimal point. This movement will provide the CPU enough reel tachometer pulses to determine a valid reel radius.
- The machine powers up in BOTH mode, that is, in both NETWORK and LOCAL modes. In NETWORK mode, all transport and audio control is derived from the Serial Network Control, and in LOCAL mode transport and audio control is derived internally from the machine and the parallel Remote Control Unit. In BOTH mode, however, transport and audio control is available from either mode on a first come/first served basis.

* This function is active on ALL APR-5000 Series machines.

Meter Housing

VU Meters - illuminated;
Monitor Indicator - REPRO;
RECORD READY - OFF;
UNCAL - OFF.

ALignment (ALN) Panel

TAPE SPEED - previous power down state;
PRESET - previous power down state;
EQ STD - previous power down state.

NOTE:

- The ALN Panel will display an "EP" Preset Error code upon initial power up to indicate if the last chosen PRESET Storage Location is invalid. To correct the Error, either choose another PRESET Storage Location, or store a valid alignment in the PRESET Storage Location that has the Preset Error. Section 3.2.3 describes how to store an *** alignment into a PRESET Storage Location.

3.2 Transport and Audio Operations

The rudimentary transport and audio operations of the APR-5000 are discussed in the following paragraphs.

3.2.1 Transport Operations

The following procedure will familiarize the user with the basic transport operations of the machine through the use of the controls on the Local Control Panel. Several other important transport-related features, such as the Manual Velocity Control (MVC) mode, Vari Speed mode, and Repeat mode, are also discussed.

3.2.1.1 Basic Operation

- STEP 1 Ensure that the APR-5000 power switch is set to ON.
- STEP 2 Cover the EOT tape sensor with an opaque card. Ensure that the supply and take-up motors slowly idle (rotate in opposite directions).
- STEP 3 Spin the Timer Roller counter-clockwise and ensure that the time in the TAPE TIME Display increments. Spin the Timer Roller clockwise and ensure that the time in the TAPE TIME Display decrements.

- STEP 4** Remove the opaque card and thread a reel of tape onto the machine as shown in Figure 3-2. Ensure that the frames decimal point in the TAPE TIME Display extinguishes to indicate that a valid radius has been established.

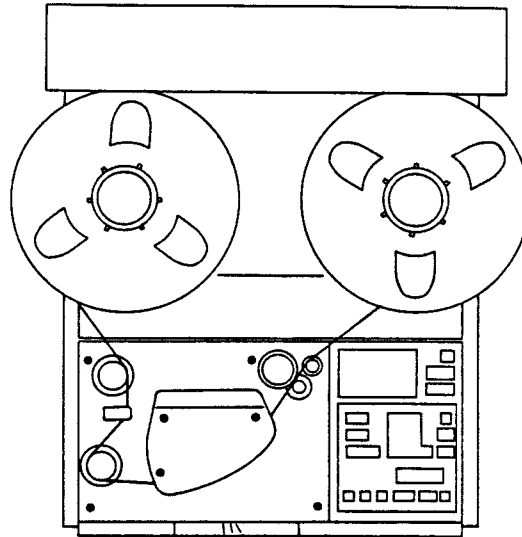


Figure 3-2. Tape Path

- STEP 5** Press PLAY. Ensure that the PLAY key indicator illuminates, the shields ascend, the pinch roller engages with the spinning capstan motor, and that the machine plays the tape across the heads.
- STEP 6** Press FWD. Ensure that the FWD key indicator illuminates, the lifters come forward, and that the tape accelerates to fast speed in the forward direction.
- STEP 7** Press LIFTER DEFEAT. Ensure that the LIFTER DEFEAT key indicator illuminates, and that the lifters retract. Press the key again and ensure that the key indicator extinguishes and the lifters come forward to their original position.
- STEP 8** Press SHIELD DEFEAT. Ensure that the SHIELD DEFEAT key indicator illuminates, and that the shields descend. Press the key again and ensure that the key indicator extinguishes and the shields ascend to their original position.
- STEP 9** Press REW. Ensure that the REW key indicator illuminates, and that the tape accelerates to fast speed in the rewind direction.

- STEP 10** Press STOP. Ensure that the STOP key indicator illuminates, the tape decelerates, stops, and the lifters retract.
- STEP 11** Press EDIT. Ensure that the EDIT key indicator illuminates, and that the reel tensions become relaxed.
- STEP 12** Press PLAY. Ensure that the take-up reel is motionless as the tape is played across the heads and dumped off the right side of the machine.
- STEP 13** Press STOP. Ensure that the play motion of the tape ceases.
- STEP 14** Press STOP again. Ensure that the EDIT key indicator extinguishes and that the reel tensions are restored.

3.2.1.2 Use of the MVC Wheel *adjustment for direction not for sensitivity -*

When the Manual Velocity Control (MVC) wheel is activated (by the touch of a finger), the MVC wheel can be used to Shuttle the tape in either a Rewind or Fast Forward direction.

When the wheel is at rest, there should be no movement of the reels. Turning the wheel more to the left increases the Rewind velocity of the tape, while turning it more to the right increases the Fast Forward velocity of the tape.

The MVC wheel can also be used to change the adjustment of the Vari Speed function, as described in the following paragraphs.

3.2.1.3 Vari Speed Mode

The VARI SPEED key enables the nominal play speed of the machine to be varied by +/- 50%. The VARI SPEED key indicator has three states, off, flashing, and on.

The machine runs at the nominal play speed, regardless of any Vari Speed entries, when the key indicator is off.

Pressing the VARI SPEED key once enters Direct Entry mode and causes the key indicator to flash. In this mode, the desired play speed variation percentage is entered via the numeric keypad, and this percentage is shown in the LOCATE TIME Display. Any entered value greater than +50% automatically defaults to +50%, and any value less than -50% defaults to -50%.

Pressing the VARI SPEED key a second time enters Execute/Manual Entry mode and causes the key indicator to illuminate solidly. In this mode, the nominal play speed is deviated by the percentage entered in Direct Entry mode. It is important to note that the nominal play speed will not vary until the machine is in Execute/Manual Entry mode.

In addition, Execute/Manual Entry mode allows the MVC Wheel to be used to deviate the nominal play speed percentage within the +/-50% deviation limits. Turning the MVC wheel to the left reduces the play speed, while turning it to the right increases the play speed. This is convenient for fine tuning the desired amount of speed variation.

Storage Location 41 (Ips/Semitone VARI SPEED Display Select) can alter the display information in the LOCATE TIME Display as follows:

Storage Location 41 = 0

Percentage of play speed deviation is displayed.

Storage Location 41 = 1

The Inches Per Second (ips) and Semitone value of play speed deviation is displayed. The semitone values are then displayed in increments of 0.25 semitones.

Pressing the VARI SPEED key a third time extinguishes the key indicator.

3.2.1.4 Repeat Mode

When the REPEAT key is pressed on the APR-5000, the machine locates to the time value stored in Memory Location (28) and automatically goes into Play. The machine remains in Play until the time value stored in Memory Location (29) is reached, at which time the machine stops and locates back to the time value in Memory Location 28 and goes into Play again, continuing this loop ad infinitum until the STOP key is pressed or power is removed from the machine.

It is important to note that the time value stored in Memory Location 29 must be positive with respect to the time value stored in Memory Location 28 in order for Repeat mode to function.

3.2.2 Audio Operations

The following procedure will familiarize the user with the basic audio operations of the machine through the use of the controls on the Meter Bridge and the Local Control Panel. Several other important audio-related features, such as Spot Erase, External RECORD READY and SYNC/REPRO Switching Control, and PRESET Storage, are also discussed.

3.2.2.1 Basic Operation

- STEP 1** Ensure that the power switch is set to ON, and load a reel of tape onto the machine.
- STEP 2** Press the RECORD READY key for each channel on the Meter Bridge Panel, ensuring that each key indicator illuminates and that the amber RECORD READY LEDs on the Meter Housing illuminate solidly.
- STEP 3** Press the SYNC key for each channel on the Meter Bridge Panel, ensuring that each key indicator illuminates solidly.
- STEP 4** Press PLAY and REC simultaneously. Ensure that the PLAY and REC key indicators are illuminated on the and on the Local Control Panel;
- Ensure that the red ERASE and BIAS LEDs on the Meter Bridge Panel are illuminated.
- STEP 5** Press STOP. Ensure that the PLAY and REC key indicators and the red ERASE, and BIAS LEDs all extinguish.
- STEP 6** Press the RECORD READY key for each channel on the Meter Bridge Panel, ensuring that each key indicator extinguishes along with the amber LEDs on the Meter Bridge.
- STEP 7** Press ALL on the ALN Panel. Ensure that ALL appears in the ALN Status Display.
- STEP 8** Press ALL on the ALN Panel. Ensure that ALL is cleared from both Status Displays, and that the flashing amber LEDs on the Meter Housing extinguish.

3.2.2.2 Spot Erase

When the SPOT ERASE key is pressed, Spot Erase mode becomes armed, providing that there is at least one channel in Record Ready mode.

Pressing the RECORD key then causes the channels in Record Ready mode to enter Spot Erase mode. The program material on those channels will be erased as the tape is manually moved across the erase head. In this mode, ONLY the Erase head is active. The record/bias signal is not routed to the Sync/Record head as in a normal Record mode.

Pressing the STOP key halts the erase current to the erase head but leaves Spot Erase mode armed, thereby allowing for additional spot erasures to be performed on another section of the tape, if desired. Pressing the SPOT ERASE key again will then disarm Spot Erase mode.

*come out
of erase
while
the tape
is moving -*

3.3 Audio Alignment

The machine is factory aligned using a reference fluxivity of 250nW/m and 3M Scotch 226 tape. Complete Input, Playback, and Record alignment procedures can be found in Section 6.6 of this manual.

3.3.1 PRESET Storage

The PRESET keys can be used to store three separate audio alignments per speed, per headstack.

To arm the Preset store function, hold down the CONTROL key and press the STORE key. The key indicator LED on the STORE key will illuminate solidly. Then, pressing any one of the three PRESET keys erases the previously stored parameters in that PRESET Storage Location and replaces it with the current parameter values of all channels.

Pressing any of the three PRESET keys recalls the parameter values that have been stored in that Storage Location, and illuminates the key indicator solidly. The PRESET key indicator will remain illuminated until the value of any of the parameters is changed or another PRESET Storage Location is selected.

NOTE: It is important to note that the hexadecimal parameter values must be stored into one of the PRESET Storage Locations before switching speeds or powering the machine down, or else those values will not be stored.

3.4 Time Code Operations

The APR-5000 is capable of performing a wide variety of time code generation and synchronization operations. These operations are discussed in the following paragraphs. Detailed background information regarding SMPTE time code standards can be found in Appendix C of this manual.

It is important to note that the machine must be in TIME CODE DISPLAY mode for these features to operate properly. For more detailed information on the time code circuitry, refer to Figure 4-3 and the collaborating text in Section 4 of this manual.

3.4.1 Time Code Generation

The APR-5000 is capable of recording time code onto the dedicated time code track through the use of the TC GEN key on the Local Transport Control Panel. The time code can originate from either an externally input source or from the internally derived clock signal. The TC GEN key has three mutually exclusive states, each of which corresponds to a specific type of external or internal time code generation. Refer to the chart in Table 3-1.

TC GEN INDICATOR	TIME CODE REFERENCE	TIME CODE DATA
OFF (Power-up default)	EXTERNAL As selected in Storage Location 37 0 = LTC DATA 1 = VITC DATA	EXTERNAL
FLASHING	EXTERNAL As selected in Storage Location 37 0 = LTC CLOCK 1 = VITC CLOCK	INTERNAL START POINT
ON	INTERNAL	INTERNAL START POINT

Table 3-1. Time Code Generator Modes

It is important to note that, before recording any external or internal time code onto the time code track, the machine must be in TC DISP mode.

Also, ensure that the time code reference signal is recognized by the machine as valid by observing the decimal points in the TAPE TIME Display of the Local Transport Control Panel, as follows:

Hours decimal point = Valid Video Reference Signal
Minutes decimal point = Valid Master time code
Seconds decimal point = Valid Slave Time Code

3.4.2 Auto Time Code Mode

Storing a 1 in Memory Location 30 enables Auto time code mode. This allows the machine to identify the time code format of the time code on a tape being played or an externally input time code signal.

If a tape with time code on it is played when this Memory Location is enabled, the machine will identify the time code format and automatically set Memory Locations 31 and 32 to reflect the format. When external time code is being input to the machine, the format of that external source will also automatically be stored into Memory Locations 31 and 32, providing that the TC GEN key is in one of the two external indicator modes, Flashing or On.

It is also important to note that Memory Location 37 must also be programmed manually by the user to reflect the type of the external time code, with 0 = LTC and 1 = VITC.

3.4.3 External Time Code Recording

Before recording external time code onto the time code track, Memory Location 37 must be set to indicate what type of time code is being input to the machine, with 0 = LTC, 1 = VITC. LTC must be input to the LTC IN XLR connector on the rear of the machine, and VITC must be input to the VIDEO IN BNC connector.

Memory Locations 31 and 32 must also be set to reflect the format of the incoming time code signal. Memory Location 31 must be set as follows:

0 = SMPTE
1 = EBU
2 = FILM

Memory Location 32 must be set as follows:

0 = SMPTE NDF, EBU, FILM
1 = SMPTE DF

Storing a 1 in Memory Location 32 automatically sets Memory Location 31 to 0, and storing a 1 or 2 in Memory Location 31 automatically sets Memory Location 32 to 0, thereby ensuring that a valid time code format is always selected. Storing a 1 in Memory Location 30 sets the machine in Auto time code mode, whereby the machine identifies the format of the external reference and automatically programs Memory Locations 31 and 32 to reflect the format.

When the TC GEN key indicator is off, the time code recorded on the time code track will be the externally input time code source, with the time value of the external data used as the starting point reference.

When the TC GEN key indicator is flashing, the time code recorded on the assigned time code track will be the external time code source, but the starting point time value is programmed by the user. The desired starting point is entered into the LOCATE TIME Display and transferred to the TAPE TIME Display using the TRANSFER UP Arrow key. The time code recorded on the assigned time code track will then start its count at the programmed time value, independent of the time value of the external input.

It is important to note that the channel assigned as the time code track must be in Record Ready mode in order to program the desired starting point into the LOCATE TIME Display.

3.4.4 Internal Time Code Recording

When the TC GEN key indicator is on, the time code recorded on the time code track will be generated by the internal time code clock signal. The time value of the starting point is programmed by the user in the same manner previously described for external generation.

The time code type recorded on the tape will be always be LTC, as the APR-5003V does not generate VITC. The format of the time code will be determined by the contents of Memory Locations 31 and 32. Memory Location 31 should be set as follows:

0 = SMPTE
1 = EBU
2 = FILM

Memory Location 32 should be set as follows:

0 = SMPTE NDF, EBU, FILM
1 = SMPTE DF

Storing a 1 in Memory Location 32 automatically sets Memory Location 31 to 0, and storing a 1 or 2 in Memory Location 31 automatically sets Memory Location 32 to 0, thereby ensuring that a valid time code format is always selected.

***** NOTE *****

It is important to note that the SMPTE time code produced by the internal time code clock is generated at 30 Fr/s, with the internal crystal reference of all time code formats accurate to +/- 50 ppm. If SMPTE DF is required at the NTSC rate of 29.97 Fr/s, it is advisable to use an external reference that produces said frame rate.

differential line out

3.4.5 Analog/RS422-Type Time Code Output

When the internal time code generator is selected (TC GEN key indicator on) and the machine is in Record, the time code format as determined by Memory Locations 31 and 32 is made available in differential analog form for external use at the LTC OUTPUT XLR connector on the rear of the machine.

Where RS422-type output is desired, remove jumpers JU1 and JU3 on the CNX (or CNX-II) board and install them onto jumpers JU2 and JU4. (Refer to Figure 3-2.)

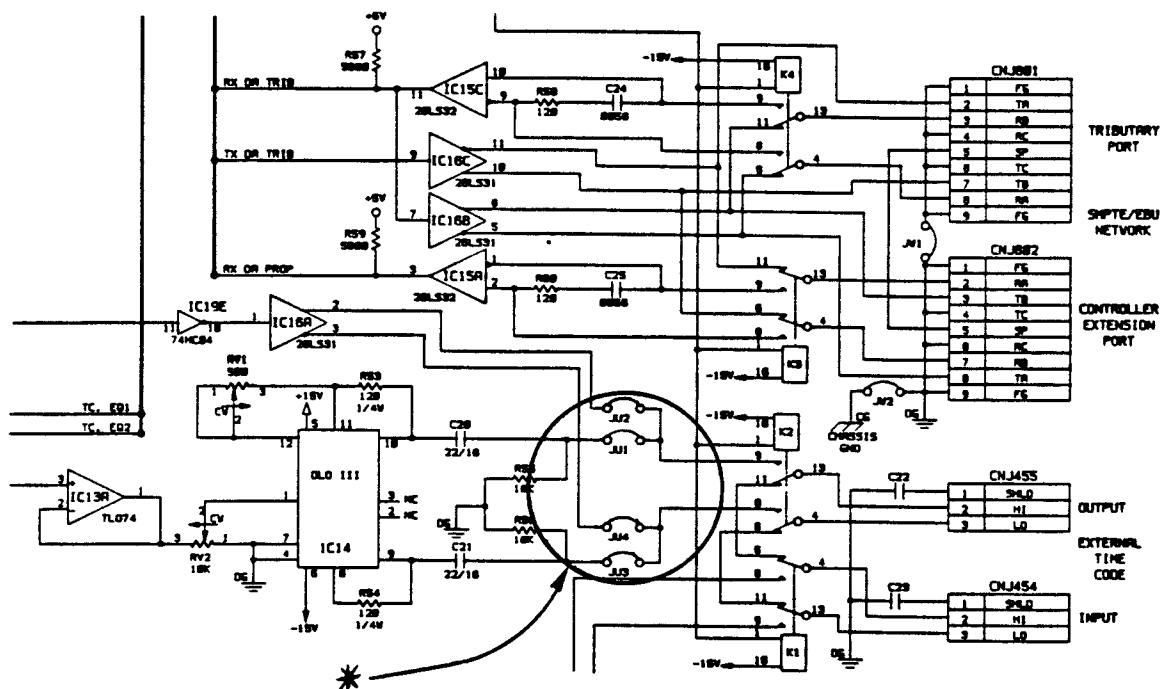


Figure 3-2. Location of Jumper Blocks on CNX Board

3.4.6 Time Code Synchronization

Time code recorded onto the time code track can be used to synchronize the machine to an external Time Code source, where either the machine follows the external source (Slave mode) or the external source follows the machine (Master mode).

The decimal points in the TAPE TIME display of the Local Transport Control Panel are used to indicate the validity of the following signals:

Hours decimal point = Valid Video Reference Signal
Minutes decimal point = Valid Master Time Code
Seconds decimal point = Valid Slave Time Code

3.4.6.1 Chase/Lock

Chase/Lock mode allows the machine to synchronize to an external source in Slave mode, provided that the time code recorded on tape is of the same type and format as that of the external source.

Before initiating Chase mode, Memory Location 37 must be set to indicate what type of time code is being input to the machine, with 0 = LTC, 1 = VITC. LTC must be input to the LTC IN XLR connector on the rear of the machine, and VITC must be input to the VIDEO IN BNC connector. The format of the external time code source must also be programmed into Memory Locations 31 and 32, either manually or automatically by storing a 1 in Memory Location 31 to enable Auto time code mode. Please refer to Section 3.4.4 for information on programming Memory Locations 31 and 32.

Once the Memory Locations have been properly set, pressing the CHASE key on the Local Transport Control Panel initiates Chase mode. The CHASE key indicator will flash while the machine is establishing Lock and will illuminate solidly when the machine is locked to the external source. Lock will be data dependent, plus or minus any offset which might be stored in Memory Locations 00 (Synch Offset, Frames) and 98 (Sub-frame Offset, bits). The machine will stay locked to the external source for a maximum drop out length of two seconds before it unlocks.

3.4.6.2 Offset

The machine may be programmed to Chase/Lock ahead or behind an external source in Slave mode by storing the desired amount of offset time into Memory Location 00.

Synchronization Offset can be adjusted to the bit level through the use of Memory Location 98. When this Memory Location is recalled, turning the MVC Wheel clockwise or counter-clockwise changes the modulo 80 bit count of the time code frame offset up or down accordingly. It should be noted that adjustment past the modulo 80 bit count of the time code word will result in an appropriate underflow or overflow of the frames offset resolution as stored in Memory Location 00.

3.4.6.3 Offset Calculation

Recalling Memory Location 99 captures the current offset between the machine and an external source, and displays it in the LOCATE TIME Display. Pressing STORE 99 then stores the calculated offset into Memory Location 00, since Memory Location 99 does not have a storage feature of its own. The offset capture will be determined by the last valid time code values read by the CPU from the playback circuit and the external circuit.

3.4.6.4 Resolve on Play

Location 39 - never have a 1

The Resolve on Play feature allows the PLAY key to be used to initiate data independent synchronization of the machine to an external LTC, video signal, or tone reference. To enable this feature, Memory Location 39 must be set to a 1 and Memory Location 37, Establish Lock Reference, must be set as follows:

0 = LTC INPUT
1 = VIDEO SIGNAL or TONE INPUT

Once the Memory Locations have been properly set, pressing the PLAY key initiates Resolve on Play mode. The CHASE key indicator will flash while the machine is establishing Lock and will then illuminate solidly when the machine is locked to the external source (providing that the external input is capable of resolving to the time code on the tape, as derived from Tables 3-2 and 3-3). One of the most interesting applications of this feature is the machine's ability to resolve a 60 Hz input tone reference to 24 Fr/s Film time code, as shown in Table 3-3.

The $\pm 0.1\%$ and -0.1% resolve percentages listed in Tables 3-2 and 3-3 indicate the deviation from the nominal recorded tape speed which the transport runs at during Resolve on Play mode. It should be noted that operation of the machine to other more substantially mis-matched clock rates during Resolve on Play mode will not provide reliable operation.

APR-5003V

INPUT SIGNAL	TIME CODE ON TAPE			
	SMPTE NDF	SMPTE DF	EBU	FILM
LTC @ 30 f/s	Resolve	+0.1%	n/a	n/a
60 Hz NTSC B _W Video	Resolve	+0.1%	n/a	Resolve*
LTC @ 29.97 f/s	-0.1%	Resolve	n/a	n/a
59.54 Hz NTS Color Video	-0.1%	Resolve	n/a	-0.1%*
LTC @ 25 f/s	n/a	n/a	Resolve	n/a
50 Hz PAL/SECAM Video	n/a	n/a	Resolve	n/a
LTC @ 24 f/s	n/a	n/a	n/a	Resolve

*NOTE: One of the most interesting applications of RESOLVE ON PLAY is the ability to resolve 60 Hz input reference signals to the 24 f/s Film Time Code, by maintaining a 4.5 Time Code to reference signal resolving ratio.

Table 3-2. Resolve Capabilities with LTC Input

APR-5003V

INPUT SIGNAL	TIME CODE ON TAPE			
	SMPTE NDF	SMPTE DF	EBU	FILM
LTC @ 30 f/s	Resolve	+0.1%	n/a	n/a
60 Hz NTSC B _W Video	Resolve	+0.1%	n/a	Resolve*
LTC @ 29.97 f/s	-0.1%	Resolve	n/a	n/a
59.54 Hz NTS Color Video	-0.1%	Resolve	n/a	-0.1%*
LTC @ 25 f/s	n/a	n/a	Resolve	n/a
50 Hz PAL/SECAM Video	n/a	n/a	Resolve	n/a
LTC @ 24 f/s	n/a	n/a	n/a	Resolve

*NOTE: One of the most interesting applications of RESOLVE ON PLAY is the ability to resolve 60 Hz input reference signals to the 24 f/s Film Time Code, by maintaining a 4.5 Time Code to reference signal resolving ratio

Table 3-3. Resolve Capabilities with Video Signal/Tone Input

3.4.6.5 Acceleration Allowance

Compensate for acceleration of VTR

The Acceleration Allowance feature allows the difference between the starting ballistics of the machine and a those of a parked Master to be adjusted and compensated for, thereby optimizing Chase/Lock synchronization.

Memory Location 50 is used to adjust the distance at which the machine parks ahead of the Master's last known position, with a maximum time value of five seconds minus one frame allowed. Setting the value to zero causes the machine to default to the intrinsic software time value. It should be noted that this Memory Location is volatile, and its contents will not be retained when the machine is powered down.

3.4.6.6 Burst Time Code

Some external synchronizers and readers are unable to interpret the interpolated time code that the machine outputs during high speed wind modes. Enabling the Burst Time Code feature provides accurate time position information over an unlimited wind speed range for the external device, thereby simplifying the external device's task of determining tape position and stopping position at high wind speeds.

Storing a 1 in Memory Location 35 enables the Burst Time Code feature. High speed wind time code is then sampled once every fifteen frames by the CPU before it is output to the external device. This presents a time code signal to the external device that appears to be in Play mode, thereby allowing it to read the time code.

When the machine reaches its stopping position, a 30 frame "burst" of the actual stopping position is output, thereby assuring frame-accurate lock between the machine and the external device.

3.4.6.7 Control Track Follow

The APR-5003V can Chase to the externally output Control Track of a VTR if that VTR is unable to provide valid time code at high speed wind modes.

In order for this function to operate, the Control Track pulse output of the VTR must be input to pin 38 of the 50-pin Parallel Port connector on the rear of the machine, and the External Direction Sense output of the VTR must be input to pin 37 of the Parallel Port connector. Also, Memory Location 46 must be set to the appropriate External Direction Sense of the incoming Control Track, to wit:

- 0 = Normal high speed time code CHASE
- 1 = Direction sense low (true) for reverse
- 2 = Direction sense low (true) for forward

When the machine is synchronized in Slave mode to the VTR and the VTR goes into high speed wind mode, the machine will Chase to the one pulse per frame Control Track pulse output of the VTR. The machine will re-lock to the VTR once valid time code is again provided.

3.5 Editing Operations

The APR-5000 is capable of performing many sophisticated editing operations designed to meet a wide variety of audio and video tape editing needs. The machine may be programmed for either manual or triggered Edit execution, five Edit Storage Registers are provided.

3.5.1 Programming Manual Edits

A Programed Edit may be executed manually or triggered from an external source. It is important to note that the time code track is prohibited from going into Record during a manually executed Programed Edit or an externally Triggered Edit.

The following Memory Locations are used in the execution of a Programed Edit:

- 01 EDIT IN POINT
- 02 EDIT OUT POINT
- 91 EDIT IN POINT, BIT RESOLUTION
- 92 EDIT OUT POINT, BIT RESOLUTION
- 51 PREROLL DURATION *⇒ like to see with least 5 secs.*
- 52 POSTROLL DURATION *- 2 secs default*

*acc panel is 10
- set to 10 secs.*

3.5.1.1 Edit In/Out Points

When TC DISP mode is activated, the Edit In/Out Points can be programmed into their respective Memory Locations with resolution down to the time code frame, and, if necessary, to the individual bit of the time code frame.

To set the Edit In Point, store the desired punch-in time into Memory Location 01. To set the Edit Out Point, store the desired punch-out time into Memory Location 02. It is important to note that the time value stored in Memory Location 02 must be positive with respect to the time value stored in Memory Location 01, and must not exceed an absolute value of twelve hours.

In applications where the Edit In Point must be accurate to an individual bit of the time code frame, recall Memory Location 91 and store the desired bit number. In applications where the Edit Out Point must be accurate to an individual bit of the time code frame, recall Memory Location 92 and store the desired bit number.

3.5.1.2 Preroll and Postroll Duration

Preroll Duration is the amount of time that the machine is in Play before the Edit In Point of a Programed Edit is executed, and Postroll Duration is the amount of time that the machine remains in Play after the Edit Out Point of a Programed Edit has been executed, as shown in Figure 3-3.

The Preroll Duration has a default setting of ten seconds, while the Postroll Duration has a default setting of two seconds. To program the Preroll Duration, recall Memory Location 51 and store the desired Preroll time. To program the Postroll Duration, recall Memory Location 52 and store the desired Postroll time.

3.5.2 Executing Manual Edits

Once the Edit In and Out Points and the Preroll and Postroll Durations have been programed, Preview, Edit or Review mode may then be executed. It is important to note that the assigned time code track is not allowed to go into Record during a manually executed Programed Edit.

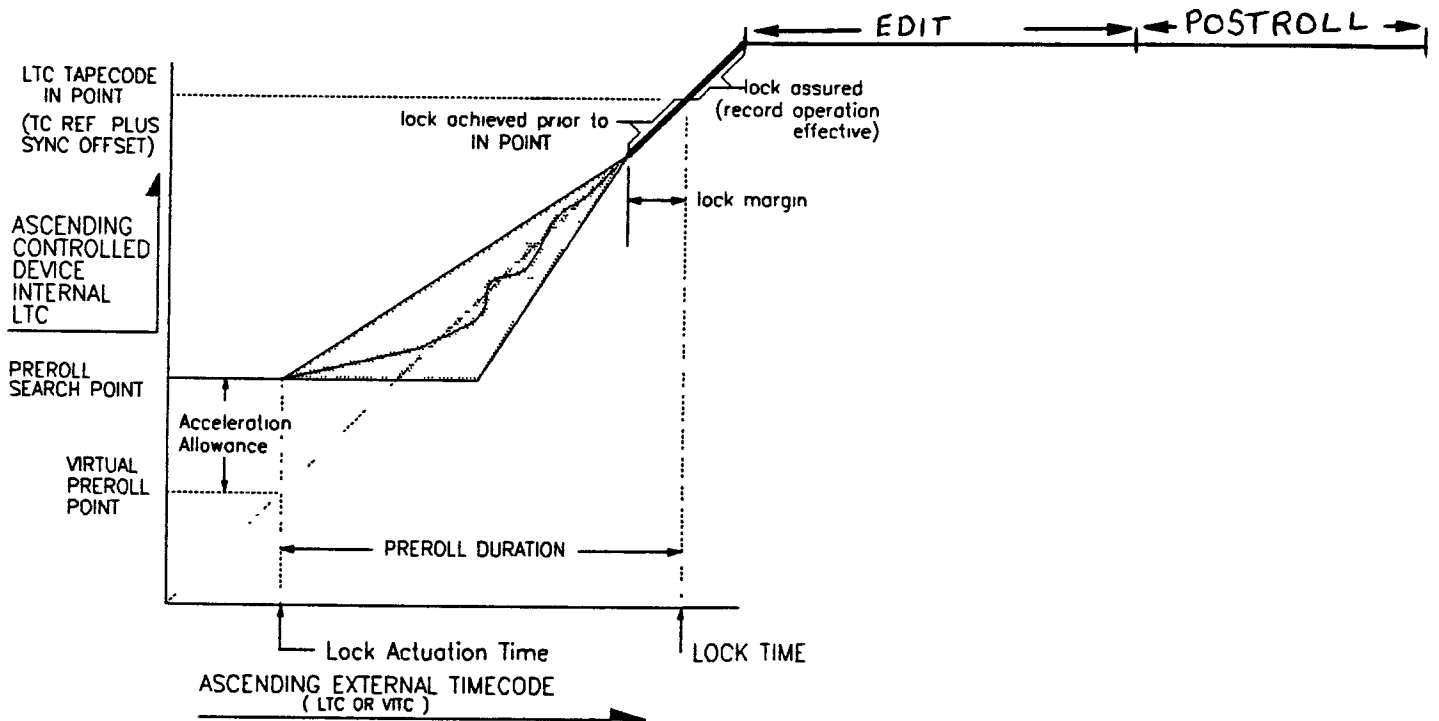


Figure 3-3. Preroll and Postroll Durations

3.5.2.1 Preview

Preview mode allows for the rehearsal of the Programed Edit without the machine actually going into Record.

When the PREVIEW Storage Location (95) is set to a 1, the machine will locate to the preassigned preroll position. Once at this position, the PLAY key will flash.

Pressing the PLAY key then causes the machine to imitate the Programed Edit, with all channels monitored from the Sync head. Then, at the Edit In Point, those channels which are in Record Ready switch to Input so that the new program material may be rehearsed over those channels. At the Edit Out Point, all the channels switch back to Sync mode and the machine continues to Play for the amount of time programed in the Postroll Duration.

3.5.2.2 Edit

Edit mode will actually execute the Programed Edit, with those channels in Record Ready going into Record mode.

When the EDIT Storage Location (96) is set to a 1, the machine locates to the Edit In Point minus the Preroll Duration, parking there with the PLAY and RECORD keys flashing.

Pressing the PLAY key then causes the machine to initiate the Programed Edit, with all channels monitored from the Sync head. Then, at the Edit In Point, those channels which are in Record Ready go into Record so that the new program material is then recorded onto those channels. At the Edit Out Point, all the channels in Record drop out of Record and the machine continues to Play for the amount of time programed in the Postroll Duration.

3.5.2.3 Review

Review mode will play back the previously executed Edit, so that the results may be monitored.

When the REVIEW Storage Location (97) is set to a 1, the machine locates to the Edit In Point minus the Preroll Duration, parking there with the PLAY key flashing.

Pressing the PLAY key then causes the machine to play back the programed edit, with all channels monitored from the Repro head. The machine continues to play and then stops at the end of the Postroll Duration.

3.5.3 Programming Triggered Edits

A Programed Edit may also be executed by using an external reference to trigger the desired Edit mode.

The Edit In and Out Points and the Preroll and Postroll Durations must first be programed as described for a Manual Edit in Section 3.5.1. In addition, a 1 must be stored in Memory Location 43 to enable the Triggered Edit Operation, and the following Memory Locations must be programed:

- 37 ESTABLISH LOCK REFERENCE
- 38 MAINTAIN LOCK REFERENCE

3.5.3.1 Establish Lock Reference

Memory Location 37 must be set to the type of external time code reference that the machine will be establishing synchronization to during the Preroll Duration portion of the Triggered Edit. It should be set as follows:

- 0 = LTC
- 1 = VITC, video signal, or tone

3.5.3.2 Maintain Lock Reference

Memory Location 38 must be set to select the external reference that the machine will maintain synchronization to once the Edit In Point of a Triggered Edit has been reached.

Data dependent synchronization refers to the machine maintaining lock to the exact time value of the ascending external reference during the Triggered Edit. Data independent synchronization refers to the machine maintaining lock to the sync pulses instead of the exact ascending time value of the external reference during the Triggered Edit. Memory Location 38 should be set as follows:

- 0 = LTC, data independent
- 1 = LTC, data dependent
- 2 = Video signal or tone, data independent
- 3 = VITC, data dependent

3.5.4 Executing Triggered Edits

Once all of the Memory Locations required to perform a Triggered Edit have been programed, the desired Edit mode may then be selected for the Triggered Edit.

3.5.4.1 Preview, Edit, and Review

The Preview, Edit, and Review modes perform exactly the same functions during a Triggered Edit as they do during a Manually executed edit. Selecting the Preview, Edit, or Review modes for a Triggered Edit causes the machine to locate to the Edit In Point minus the Preroll Duration and park there with the PLAY key flashing, exactly as in a Manual Edit.

However, instead of pressing the PLAY key to initiate the mode, the machine waits for the time value of the external reference to reach the time value of where the machine is parked, at the start of the Preroll Duration. Once this time

is reached, the Programed Edit is then executed. It is important to note that any Synchronization Offset stored in Memory Locations 00 or 98 will effect the execution start time of the Triggered Edit by the amount of the amount of the offset.

Synchronization is established during the Preroll Duration in accordance with the external time code type, as stored in Memory Location 37, so that prior to the Edit In Point synchronization is assured. The external reference should be presented to the machine for a reasonable amount of time during the Preroll Duration. If for any reason synchronization is not established prior to the Edit In Point, the Triggered Edit operation will be aborted before any Record editing functions are executed.

After the Edit In Point is reached, synchronization is maintained as specified by the reference stored in Memory Location 38.

3.6 Memory Locations

The Memory Locations are used to store and enable a wide variety of machine parameters and functions. Information regarding Default Settings, Recalling and Storing, and Storage Registers 03-27 is provided, as well as a manual reference index.

3.6.1 Default Settings

The machine is factory-shipped with all of the Memory Locations set to zero, with the exception of Memory Location 51, Preroll Duration, and Memory Location 52, Postroll Duration, which have default settings of ten and two seconds, respectively.

3.6.2 Recalling and Storing

To recall a Memory Location, press the RCL key and enter the two-digit number of the Memory Location. The contents of that Memory Location will then be shown in the LOCATE TIME Display.

If it is desired to store a new number into that Memory Location, enter the new number on the keypad and then press the STO key.

3.6.3 Storage Registers 03-27

Memory Locations 03-27 may be used to store any time values that might be beneficial to recall for locating, editing, and other purposes.

3.6.4 Memory Location Reference

Table 3-4 lists where the operational and functional descriptions can be found in this manual for all of the Memory Locations.

MEMORY LOCATIONS	REFERENCE
00 SYNCHRONIZATION OFFSET, FRAME RESOLUTION	SECTION 3.4.6.2
01 EDIT IN POINT, FRAME RESOLUTION	SECTION 3.5.1.1
02 EDIT OUT POINT, FRAME RESOLUTION	SECTION 3.5.1.1
03-27 STORAGE REGISTERS	SECTION 3.6.3
28 REPEAT START TIME	SECTION 3.2.1.4
29 REPEAT STOP TIME	SECTION 3.2.1.4
30 AUTO TIME CODE MODE	SECTION 3.4.2
31 TIME CODE FORMAT	SECTION 3.4.3
32 SMPTE DROP FRAME FORMAT	SECTION 3.4.3
35 BURST TIME CODE	SECTION 3.4.6.6
37 ESTABLISH LOCK REFERENCE	SECTION 3.4.6.1
38 MAINTAIN LOCK REFERENCE	SECTION 3.4.6.1
39 RESOLVE ON PLAY	SECTION 3.4.6.4
41 VARI SPEED IPS/SEMITONE DISPLAY	SECTION 3.2.1.3
42 Not Used	
43 TRIGGERED EDIT OPERATION	SECTION 3.5.3/.4
44 Not Used	
45 Not Used	
46 CONTROL TRACK FOLLOW/DIRECTION SENSE	SECTION 3.4.6.7
50 ACCELERATION ALLOWANCE	SECTION 3.4.6.5
51 PREROLL DURATION	SECTION 3.5.1.2
52 POSTROLL DURATION	SECTION 3.5.1.2
53 Not Used	
54 Not Used	
60-64 Not Used	
70-74 Not Used	
91 EDIT IN POINT, BIT RESOLUTION	SECTION 3.5.1.1
92 EDIT OUT POINT, BIT RESOLUTION	SECTION 3.5.1.1
98 SYNCHRONIZATION OFFSET, BIT RESOLUTION	SECTION 3.4.6.2
99 OFFSET CALCULATION	SECTION 3.4.6.3

Table 3-4. Memory Location Reference Index

SECTION 4 TRANSPORT CIRCUIT DESCRIPTIONS

4.0 Overview

This section provides the required information for the accurate understanding and troubleshooting of the APR-5000 transport system. The transport system will be discussed as three sub-systems;

- 1) Transport Control/Interface System
- 2) Tension Servo System
- 3) Capstan Servo System

This section begins with a general block diagram discussion that illustrates the interconnect and function of the transport system as a working unit. Detailed individual circuit descriptions follow the general block diagram tutorial.

4.1 Transport System Overview

As discussed in the previous section, the transport system is segregated into three interacting sub-systems. The Transport Control/Interface System interfaces all user accessible keystroke command to the transport (and audio) system. The synchronizer is also located in this system. The built-in synchronizer handles all of the synchronizer functions of the APR-5000. The heart of the synchronizer is the CPU board which controls the local the local transport according to the soft-key selections made by the user. The Tension Servo System, under control of the Transport Control/Interface System, provides the constant tension servo loop for proper tape handling. The Capstan Servo System (which is also controlled by the Transport Control/Interface System) provides the means by which the Capstan Motor phase and speed are regulated. The following sections contribute more detailed information on the sub-system blocks. While studying Section 4.1, refer to the block diagram illustrated in Figure 4-1.

4.2 Transport Control/Interface System

This system consists of:

- 1) Manual Velocity Control (MVC) Wheel
- 2) Key Board (KBD)
- 3) Display Board (DSP)
- 4) End Of Tape (EOT) Sensor
- 5) Central Processing Unit (CPU) Board
- 6) Local/Network Transceiver (LNT) Board
- 7) Connector Interface (CNX) Board
- 8) Video/VITC Translator (VVT) Board

The operator controls the transport modes by manipulation of the transport control keys either on the parallel Remote Control Unit (RM-5010) or the local Key Board (KBD). These commands are routed to the CPU board which interprets the input data and directs the interpretation to the TIB board for reel motor and capstan servo system control. This completes the basic Control System Loop.

Advanced transport control is handled by the synchronizer section. The synchronizer, which is built into the CPU board, operates in conjunction with the following boards:

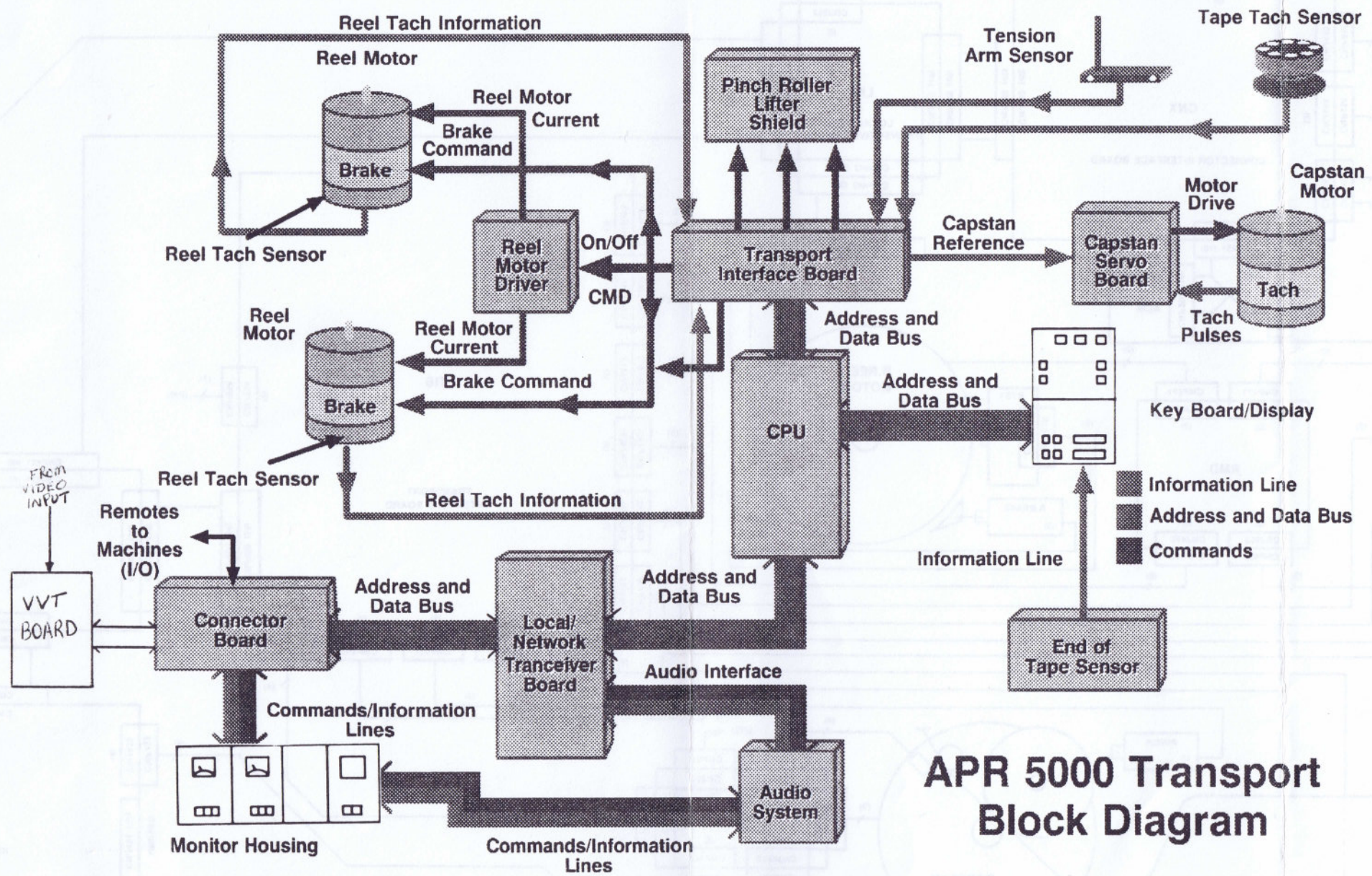
- 1) Local/Network Transceiver (LNT) Board
- 2) Connector Interface (CNX) Board
- 3) Video/VITC Translator (VVT) Board

To better understand the APR-5000 Control/Interface System, the interface signal flow will be discussed as follows:

- 4.2.1) Transport Key Panel command flow
- 4.2.2) Remote Control Unit command flow
- 4.2.3) Basic Synchronizer Operation

4.2.1 Transport Key Panel Command Flow

Keystrokes made at the Transport Key Panel (on the KBD board and the DSP board) are encoded by an 8279 (on the KBD board) and read by the CPU via the 8-bit (DB-0 through DB-7) parallel data bus. This bus cable connects the KBD board CNJ-432 (40-pin) to the CPU board CNJ-422. The KBD board provides the drive for the EOT Sensor and "houses" the EOT sensitivity adjustment circuit. The EOT Sensor command line has the global control of transport keystroke enable. The MVC wheel position/movement DC voltage is manipulated at the KBD board by RV1. The output of this circuit is a DC voltage which is routed to the CPU board via pin 2 of CNJ-422 (KBD) board.



APR 5000 Transport Block Diagram

Figure 4-1A. APR-5003V Transport Block Diagram

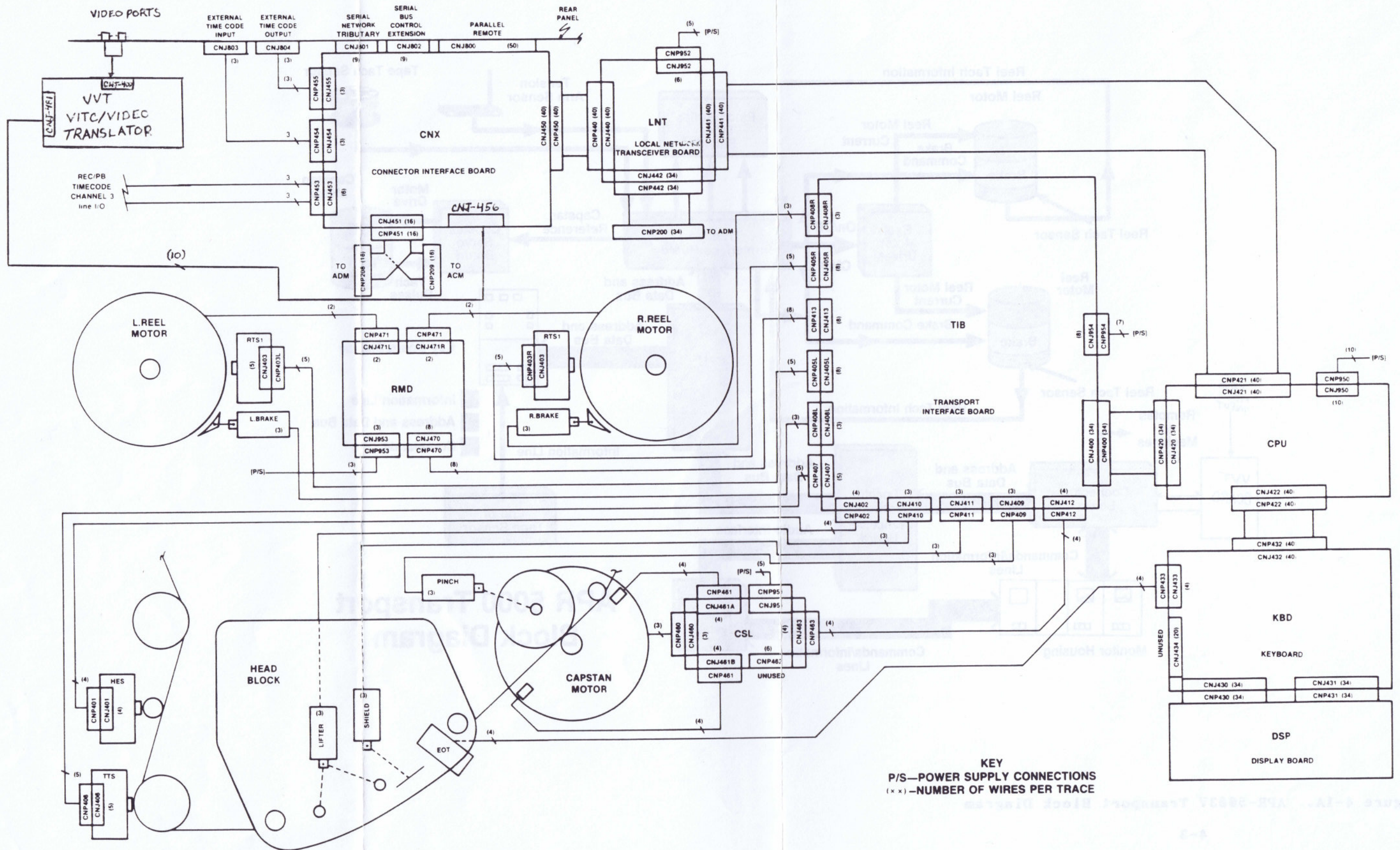


Figure 4-1B. APR-5003V Transport Interconnect Diagram

DSP BOARD KEYS	KBD BOARD KEYS
LOCAL NETWORK SHIELD DEFEAT LIFTER DEFEAT RESET(x2) LOCATE T.C. DISPLAY SPEED "TEN KEY" PAD SHIFT UP SHIFT DOWN T.C. GEN * CHASE * REPEAT VARI SPEED STORE RECALL +/- SPOT ERASE	STOP PLAY RECORD FAST FORWARD REWIND EDIT

* These keys are installed on the APR-5003 and APR-5003V units only.

Table 4-1 Transport Control Key Locations

The MVC wheel receives the enable as a result of the CPU board reading the data returning from the KBD board. When the touch sensitivity circuit is triggered (by the users finger), return line RL0 latches low (as in a key switch closure). This return line is encoded by IC14 (8279) on the KBD board and routed to the CPU board. This data word will inform the CPU that there is MVC activity and that it must "look" at the MVC LOCAL voltage for transport reel motor shuttle control.

By utilizing a Programmable Keyboard/Display Interface (8279), the KBD board can drive the Display (DSP) board. The DSP board is a simple connection board which houses the display element, and several switches, all driver/receiver circuitry is located on the KBD board. The key location chart shown in Table 4-1 lists which keys are on the KBD board and which keys are on the DSP board. The physical location of the DSP board, is at the Transport Control Panel on the front right side of the APR-5000 main unit.

4.2.2 Remote Control Unit Command Flow

The parallel Remote Control Unit (RM-5010) Transport Control commands are encoded by the 8279 (located on the CNX board). Encoded data is routed to the CPU board via the Connector Interface (CNX) board and the Local/Network Transceiver (LNT) board.

Since audio control commands can originate at the Remote Unit, the Remote Unit Audio Control command lines are connected to the audio system via the Local/Network Transceiver (LNT) board. However, the CNX board performs the absolute isolation of the internal CPU from external devices. A remote control key-stroke sequence occurs as follows:

- 1) The remote control inputs are coupled to the APR-5000 through opto-isolators and form a key matrix. The key matrix of the remote control is constantly being scanned by the 8279 (Programmable Keyboard/Display Interface) located on the CNX board (IC3). When a key is pressed on the parallel remote control, the signal that was sent out (from the 8279) to scan the key is returned to the 8279 via the return lines.
- 2) The CPU board chooses to read the 8279 (on the CNX board) by enabling the chip select line and the read line of the 8279. This action is done in the normal cycle of the CPU approximately every 1msec.
- 3) The CPU, upon reading this data from the CNX board (via the LNT board), interprets the incoming information through the use of the software program (EPROMs). For example, if the PLAY key was pressed on the remote unit the CPU will interpret the encoded data output as a PLAY command. The CPU will then issue the data necessary to illuminate the remote unit PLAY key, and the required transport control data for PLAY mode to the Transport Interface Board (TIB).

The commands from the Remote Unit Transport/Audio Function Control keys and the Local Transport Function Control keys operate the CPU on a first come first served basis.

4.2.3 Fundamentals of Synchronizer Operation

For synchronization of two or more machines to take place, there must be a common timing signal. All of the machines in a synchronization system must have this signal routed to them as a reference. Using this common reference, a machine that is synchronized will perform the following basic functions:

- Read the incoming external timing signal (time code) phase and data (if applicable).
- Read the timing signal (time code) off of the tape playing back on the machine.
- Compare these two timing signals and calculate whether a LOCK or an UNLOCK condition exists.
- If an UNLOCK condition exists, the synchronizer controller (in the case of the APR-5003V, the CPU board) will adjust the transport PLAY speed or wind mode accordingly.

With these general synchronization (sync) concepts in mind, consider an application of this type of sync system. One or more of the APR-5003V machines could be used as a high quality audio source synchronized to a video machine. With this method, the final product audio signal is of much greater quality than that of the standard audio tracks of the video machine. In addition, the possibilities of multiple tracks allows the user to be more creative with the particular piece they are developing.

An additional feature of most synchronizer systems is the ability to perform an operation known as synchronization offset. The APR-5003/5003V has the ability to perform two types of synchronization offset, Synchronization Offset (frames) and "Bit Bump" Offset. To better understand these features, let us define exactly what each term means.

Synchronization Offset (frames):

This type of offset is used when the timing of the audio signal (on the tape being played back from the APR-5003/5003V) requires a shift in time. For example, in an audio sweetening system where one or more APR-5003/5003V(s) is (are) synchronized to a video machine, the video picture must be in perfect time with the audio tracks. This "lip-sync" must be accomplished. However, the time code value of the example audio tape is not synchronous to the time code value of the video tape. The difference between the two time code values is; audio leads video by 2 seconds and 22 frames. Knowing the approximate offset of the two time code values, a Synchronization Offset of 2 seconds and 22 frames can be stored into storage register #00. This offset calculation is then automatically performed by the APR-5003/5003V machine. Depending on the configuration of multiple APR machines, this procedure may be required on all of the audio machines. Thus, the Synchronization Offset is a data dependent function of the APR-5003/5003V built-in synchronizer. This is surmised from the fact that the synchronizer of the APR-5003/5003V is calculating a time code DATA VALUE offset. The accuracy of this type of offset is limited to the frame level (33.33msec).

"Bit Bump" Offset (Sub-frame offset):

The "Bit Bump" Offset (also known as Sub-frame Offset) is calculated by the built-in synchronizer using the phase relationship of the playback time code sync pulse to the external reference time code sync pulse. With this form of offset, only the phase of the time code signals (playback and external reference) is used in the calculation. For example, in the previous explanation the offset calculation was 2 seconds and 22 frames. If this offset of 2 seconds and 22 frames is not exactly correct, an additional sub-frame offset ("Bit Bump") can be added to the calculation. This is accomplished by storing the value (00-79) of the sub-frame offset into storage register #98 (in addition to the value previously stored in register #00). After the storage of the desired value into register #98, the built-in synchronizer will offset the phase relationship of the playback time code sync to the external time code reference. This offset is done in 1/80th of a frame increments in either the positive or negative direction. This feature allows the APR-5003/5003V to offset the synchronization with 416 microsecond accuracy.

4.2.3.1 APR-5003/5003V Built-in Synchronizer Operation

The built-in synchronizer is available in the APR-5003V model only. The synchronizer feature is facilitated by the Z-8002 microprocessor circuit and software program of the APR-5003V CPU board and support circuitry.

To fully understand the operation of the synchronizer circuitry in the APR-5003V, two commonly used operation sequences will be explained. The examples that will be discussed are as shown below. For these examples, refer to the APR-5003V time code signal flow diagram in Figure 4-2.

4.2.4 APR-5003V Chase Synchronized to an external LTC source.

4.2.5 APR-5003V Chase Synchronized to an external VITC source.

4.2.4 APR-5003V Chase Synchronized to an External LTC Source

For this example, it will be assumed that the APR-5003V will be synchronizing (without an offset) to an external Longitudinal Time Code (LTC) source. The external time code source and the tape time code are assumed to be SMPTE NDF. In this example (as in all of the examples in this section), the CPU board will be performing the synchronization of the APR-5003V. This is accomplished by the Z-8002 circuit utilizing a Z-8030 (Serial Communications Controller).

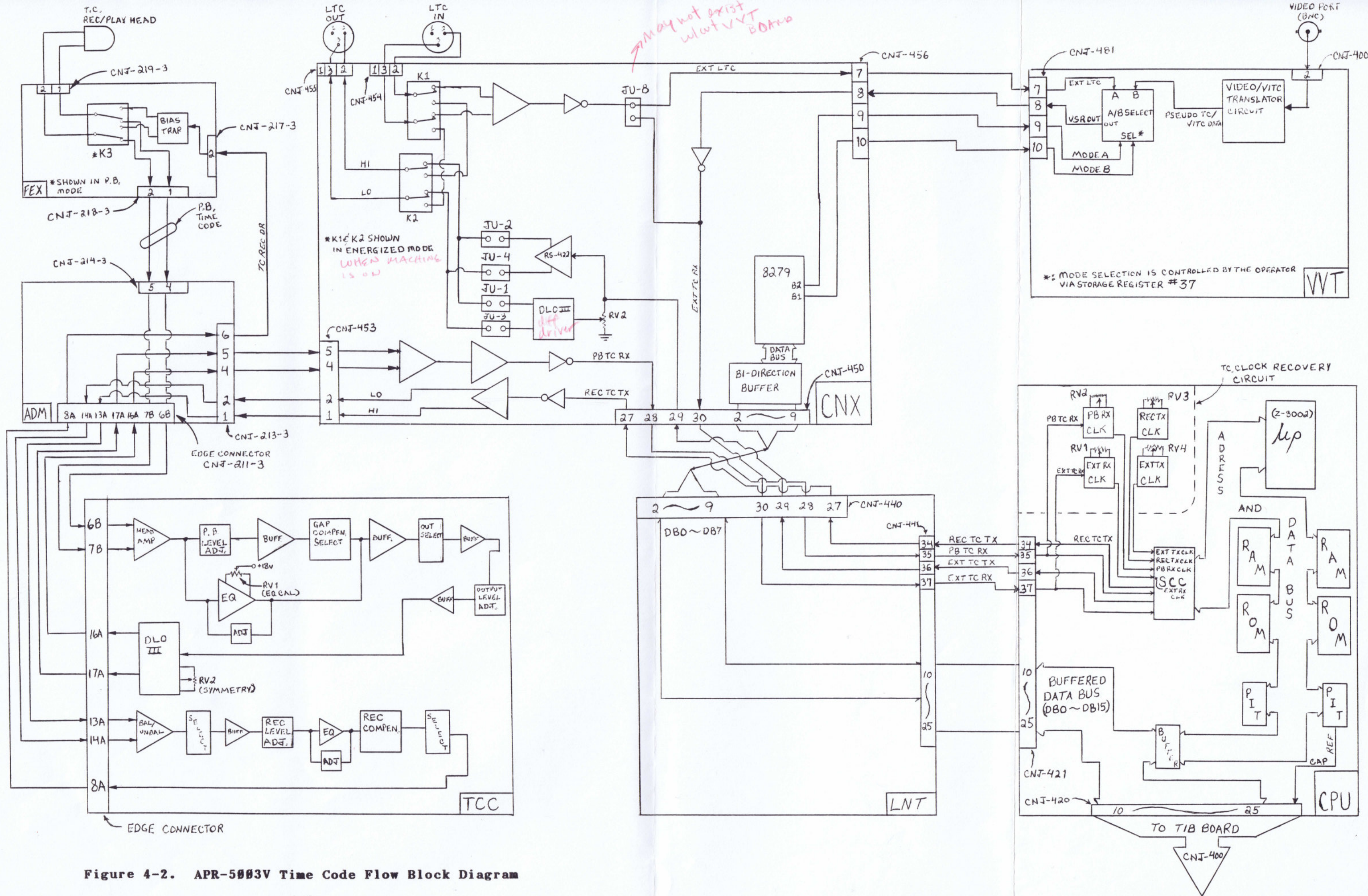


Figure 4-2. APR-5003V Time Code Flow Block Diagram

A comparison of the incoming external time code to the playback time code (off tape) is performed by the CPU circuit. The information obtained by the CPU in comparing the value of the time code within these two signals is used to control the transport. Hence, the CPU compares the two time code sources and outputs the appropriate data to the TIB (Transport Interface Board) board for transport servo system control. The set-up for the pertinent storage registers of the APR-5003V are as follows:

STORAGE REGISTER #	VALUE
00: Sync Offset, Frames	time (should be 00:00:00:00)
30: Auto TC Enable	1
31: TC Type	0 (SMPTE)
32: Drop Frame Select	(automatic selection with 30 set to 1)
35: Burst time code Enable	(activated when using another Sony analog tape machine as the external source)
*37: Establish Lock Reference Select	0 (LTC)
*38: Maintain Lock Reference Select	1 (External LTC, Data Dependent)
39: Resolve On Play	0 (Disable)
43: Triggered Edit Enable	0 (Disable)
98: BIT BUMP (Sub-frame Offset)	00-79 (should be 00)

*: To eliminate the possibility of operator error, these settings should be confirmed before the operation is attempted.

With the storage registers set as prescribed, the CPU will be prepared to perform the synchronization function of the tape time code value to the external LTC source. Refer to the block diagram in Figure 4-2.

4.2.4.1 External LTC Time Code Signal Path

The path of the external LTC time code source within the APR-5003V begins at the XLR connector on the rear panel. From the connector, the LTC signal is routed to the CNX board (CNJ-454). K1 serves as the power OFF Loop-through. When the power to the APR-5003V is turned OFF, this relay (in conjunction with K2) routes the incoming LTC time code to the LTC output connector. When K1 is in the energized state (power ON), the balanced LTC signal is converted to a single-ended TTL signal and becomes the EXT LTC signal as shown on the diagram. The jumper block (JU-8) is used to

bypass the VVT board. This jumper allows the bypass of the VVT board VSR (Video Sync Reference) OUT signal path. Hence, the VSR OUT line is connected via jumper block to the EXT LTC IN line. With the jumper block JU-8 installed the APR-5003V will only read the LTC input and storage register #37 MUST be set to a value of 0. Under normal operating conditions, this jumper is NOT installed.

The EXT LTC signal exits the CNX board at pin 7 of CNJ-456. This signal routing is necessary for the EXT LTC signal to be presented at the selector located on the VVT board. The EXT LTC signal enters the VVT board on pin 7 of CNJ-481. From this connector the EXT LTC signal is routed to the selector circuit which is controlled by the CPU (storage register #37). This selector circuit will make the final determination of which time code source (LTC, * pseudo TC, or VITC) is to be routed to the CPU board time code reader circuit.

Since the example being discussed will be using the LTC port, storage register #37 is set to a value of 0. The CPU controls the selector such that the EXT LTC IN signal is output from the VVT board as the VSR (Video Sync Reference) OUT signal. This signal is output from the VVT board via pin 8 of CNJ-481.

The selector circuit on the VVT board is directly controlled by the MODE A and MODE B command lines. These dedicated command lines are interpreted from the data bus of the CPU by the 8279 (Programmable Keyboard/Display Interface, IC3A) on the CNX board. The information stored in the register #37 mentioned earlier, is sent from the CPU board (via the data bus) to the CNX board. Hence, the 8279 on the CNX board decodes the MODE A and MODE B commands and routes them via pins 9 and 10 respectively of CNJ-456 (on the CNX board).

The VSR OUT signal from the VVT board is input to the CNX board (from the VVT board) at pin 8 of CNJ-456. From the connector, the VSR OUT signal is TTL buffered and output to the LNT board via pin 30 of CNJ-450 as the EXT TC RX signal. The LNT board receives this signal at pin 30 of CNJ-440 and simply connects this input directly to the CPU interface connector CNJ-441 (pin 37).

Upon entering the CPU board at pin 37 of CNJ-421, the EXT TC RX signal is buffered and routed to the time code clock recovery circuit and the Serial Communications Controller (SCC) IC24. The EXT TC RX time code clock recovery circuit is adjusted for optimum duty cycle (46% positive) by RV1.

*: For more information concerning the Pseudo TC signal, refer to the VVT board circuit description later in this section.

The SCC uses the timing signal developed by the time code clock recovery circuit as the receiver clock (EXT RX CLK) signal. Using the two signals (EXT TC RX and EXT RX CLK), the SCC reads the serial data content of the external time code signal. The SCC then issues an interrupt signal to the Z-8002 (microprocessor). The Z-8002 then enables the SCC to transfer data onto the parallel data bus.

4.2.4.2 Playback Time Code Signal Path

The signal path for the playback time code begins at the dedicated time code record/play head. The cables to/from the TC record/play head are connected to the FEX (Front End Transformer) board. K3 on the FEX board determines whether the head is to be used for playback or record of the time code signal on the tape. During playback K3 is energized providing a feed to the cue circuitry the playback mode. The differential playback time code signal leaves the FEX board at pins 1 & 2 of CNJ-218-3. The interconnect harness routes the playback time code signal to the ADM (Audio Mother Board). The ADM board receives this signal at pins 4 & 5 of CNJ-214-3 and performs simple signal routing to the TCC (Time Code Card) edge connector CNJ-211-3 pins 6B & 7B.

The signal routing and conditioning that occurs on the TCC card is quite similar to the CNL (ChaNneL) card. The playback signal is first routed to a pre-amplifier. This head pre-amp will unbalance the playback signal with an LM394 (matched transistor pair, instrumentation type amplifier) and 5534 differential amopliifier configuration. The unbalanced output of this stage is connected to the Digitally Controlled adjustment circuit (which is controlled by the CPU via the MST card) for playback signal level and frequency equalization. The next stage of the signal flow is the Head Gap Compensation circuit. This equalization circuit is designed to compensate for varying head types such as amorphous and 1/2-inch stereo (the same as found in a standard APR channel signal path). Adjustment of this parameter for the TCC card however, is not required since there is only one type of head that will be used for playback.

The final stage of the TCC card circuitry is the differential line output amplifier. This circuit has a symmetry adjustment (RV2) which is aligned for a symmetrical balanced output from the TCC card. The playback time code signal level at this output should be approximately +4dB. The differential playback time code signal leaves the TCC card via the edge connector pins 16A (HI) and 17A (LO).

The ADM board receives this signal from the TCC at CNJ-211-3 pins 16A & 17A. The ADM signal path routes the playback time code signal to connector CNJ-213-3 pins 4 & 5 respectively. The interconnect harness directs the playback time code signal lines to the CNX board. The playback time code signal enters the CNX board at pins 4 & 5 of CNJ-453. From this point the differential signal is connected to a differential amplifier with an unbalanced output. Next, the playback time code signal is converted to a single-ended TTL signal which is labeled PB TC RX. The PB TC RX signal is output from the CNX board to the LNT board via pin 28 of CNJ-450.

The LNT board serves as "hard wire" connection between the CNX and the CPU. The PB TC RX signal leaves the LNT board at pin 35 of CNJ-441. This signal enters the CPU board at pin 35 of CNJ-421. Once at the CPU board, the PB TC RX signal is buffered and routed to the time code clock recovery circuit and the Serial Communications Controller (SCC) IC24. The time code clock recovery circuit is adjusted (using RV2) for optimum duty cycle (46% positive). The SCC uses the timing signal developed by the time code clock recovery circuit as the receiver clock (PB RX CLK) signal. Using the two signals (PB TC RX and PB RX CLK), the SCC reads the serial data content of the playback time code signal. The SCC then issues an interrupt signal to the Z-8002 (microprocessor). The Z-8002 then enables the SCC to transfer data onto the parallel data bus.

4.2.4.3 CPU Synchronization Operation w/LTC

The Z-8002 will use the data stored in the EPROMs (Erasable Programmable Read Only Memory) to compare the external time code source signal (EXT TC RX)* to the playback time code signal (PB TC RX). The Z-8002 will then issue transport servo system control data to the TIB board. This servo system control data will vary depending on the difference between the external time code data (and phase) value and the playback time code data (and phase) value. For example, if the time code value difference is over 4 seconds, the CPU will command the transport to enter Shuttle mode to quickly ascend/descend the value of the playback time code value.

NOTE: The APR-5003V has the capability to synchronize in either a data dependent mode or a data independent (phase). Refer to information on storage register #38 in Section 3 of this manual.

* Remember, the EXT TC RX signal for this example is entering the APR-5003V from the LTC port.

This will allow a more rapid lock sequence of the playback time code value to the external time code value. When the time code value of the playback data and the external data are within 4 seconds, the CPU simply varies the CAPSTAN REF signal. This "slew" action by the capstan motor servo is the "fine adjustment" of the absolute synchronization of the playback time code data to the external time code data.

4.2.5 APR-5003V Chase Synchronized to an External VITC Source

For this example, it will be assumed that the APR-5003V will be synchronizing to an external Vertical Interval Time Code (VITC) source. The external time code source and the tape time code are assumed to be SMPTE NDF. In this example (as in all of the examples in this section), the CPU board will be performing the synchronization of the APR-5003V. This is accomplished by the Z-8002 circuit utilizing a Z-8030 (Serial Communications Controller). A comparison of the incoming external time code to the playback time code (off tape) is performed by the CPU circuit. The information obtained by the CPU in comparing the value of the time code within these two signals is used to control the transport. Hence, the CPU compares the two time code sources and outputs the appropriate data to the TIB (Transport Interface Board) board for transport servo system control. The set-up for the pertinent storage registers of the APR-5003V are as follows:

STORAGE REGISTER #	VALUE
00: Sync Offset, Frames	time (should be 00:00:00:00)
30: Auto TC Enable	1
31: TC Type	0 (SMPTE)
32: Drop Frame Select	(automatic selection with 30 set to 1)
35: Burst time code Enable	(activated when using another Sony analog tape machine as the external source)

(continued on next page)

STORAGE REGISTER #	VALUE
*37: Establish Lock Reference Select	1 (VITC)
*38: Maintain Lock Reference Select	1 (VITC Data Dependent)
39: Resolve On Play	0 (Disable)
43: Triggered Edit Enable	0 (Disable)
98: BIT BUMP (Sub-frame Offset)	00-79 (should be 00)

*: To eliminate the possibility of operator error, these settings should be confirmed before the operation is attempted.

With the storage registers set as prescribed, the CPU will be prepared to perform the synchronization function of the tape time code value to the external VITC source. Refer to the time code flow diagram in Figure 4-2.

4.2.5.1 External VITC Time Code Signal Path

The path of the external VITC time code within the APR-5003V begins at the BNC connector on the rear panel. From the connector, the VITC signal is routed to the VVT board connector (CNJ-400). The jumpers (JU-1 and JU-2) are provided for impedance matching of the input stage of the APR-5003V to the output stage of the equipment generating the video signal. Since all video playback signals exhibit some amount of jitter, the video translator circuit on the VVT board incorporates a phase lock loop circuit. This will allow the APR-5003V to lock to the incoming video signal for proper decoding of the VITC data. IC7 (CX-7913A) is the VITC/Video decoder chip. When VITC is present, this IC will decode and output the VITC code onto a four bit parallel data bus. This output data is encoded into a serial time code data flow and present this signal to the selector circuit.

NOTE: The LEDs located on the VVT board should be illuminated as follows:

DS-1 (Green): ON (Valid VITC data)
DS-2 (Red) : OFF (Video Reference Locked)

If conditions other than the previously described exist, check the quality of the video signal input to the APR-5003V at TP1 of the VVT board.

This selector circuit which is controlled by the CPU (storage register #37) will make the final determination of which time code source (LTC, * pseudo TC, or VITC) is to be routed to the CPU board time code reader circuit.

*: For more information concerning the Pseudo TC signal, refer to the VVT board circuit description at the end of this section.

Since the example being discussed will be using the VITC port, storage register #37 is set to a value of 1 and the VITC signal is output from the VVT board as the VSR (Video Sync Reference) OUT signal. This signal is in a longitudinal TTL format and output from the VVT board via pin 8 of CNJ-481.

The selector circuit on the VVT board is directly controlled by the MODE A and MODE B command lines. These dedicated command lines are interpreted from the data bus of the CPU by the 8279 (Programmable Keyboard/Display Interface, IC3A) on the CNX board. The information stored in the register #37 mentioned earlier, is sent from the CPU board (via the data bus) to the CNX board. Hence, the 8279 on the CNX board decodes the MODE A and MODE B commands and routes them via pins 9 and 10 respectively of CNJ-456 (on the CNX board).

The VSR OUT signal (as mentioned earlier in this section) is input to the CNX board (from the VVT board) at pin 8 of CNJ-456. From the connector, the VSR OUT signal is TTL buffered and output to the LNT board via pin 30 of CNJ-450 as the EXT TC RX signal. The LNT board receives this signal at pin 30 of CNJ-440 and simply connects this input directly to the CPU interface connector CNJ-441 (pin 37).

Upon entering the CPU board at pin 37 of CNJ-421, the EXT TC RX signal is buffered and routed to the time code recovery circuit and the Serial Communications Controller (SCC) IC24. The time code recovery circuit is adjusted for optimum duty cycle (as prescribed in Section 6 of this manual). The SCC uses the timing signal developed by the time code recovery circuit to interface the EXT TC RX signal to the Z-8002 parallel data bus.

4.2.5.2 Playback Time Code Signal Path

The signal path for the playback time code begins at the dedicated time code record/play head. The cables to/from the TC record/play head are connected to the FEX (Font End Transformer) board. K3 on the FEX board determines whether the head is to be used for playback or record of the time code signal on the tape. During playback K3 latches in the playback mode. The differential playback time code signal leaves the FEX board at pins 1 & 2 of CNJ-218-3. The interconnect harness routes the playback time code signal to the ADM (Audio Mother Board). The ADM board receives this signal at pins 4 & 5 of CNJ-214-3 and performs simple signal routing to the TCC (Time Code Card) edge connector CNJ-211-3 pins 6B & 7B.

The signal routing and conditioning that occurs on the TCC card is quite similar to the CNL (ChaNneL) card. The playback signal is first pre-amplified and unbalanced by an LM394 (matched transistor pair) and 5534 op-amp configuration. The output of this stage is connected to the Digitally Controlled Resistor adjustment circuit (which is controlled by the CPU) for playback signal level and frequency equalization. The next stage of the signal flow is the Head Gap Compensation circuit. This circuit was designed to accommodate for varying head types such as amorphous and 1/2-inch stereo (as found in a standard APR channel signal path). Adjustment of this parameter for the TCC card however, is not required since there is only one type of head that will be used for playback.

The final stage of the TCC card circuitry is the differential line output amplifier. This circuit has a symmetry adjustment (RV2) which is aligned for a symmetrical balanced output from the TCC card. The playback time code signal level at this output should be approximately +4dB. The differential playback time code signal leaves the TCC card via the edge connector pins 16A (HI) and 17A (LO).

The ADM board receives this signal from the TCC at CNJ-211-3 pins 16A & 17A. The ADM signal path routes the playback time code signal to connector CNJ-213-3 pins 4 & 5 respectively. The interconnect harness directs the playback time code signal lines to the CNX board. The playback time code signal enters the CNX board at pins 4 & 5 of CNJ-453. From this point the differential signal is connected to the balance/unbalance stage. Next, the playback time code signal is converted to a single-ended TTL signal which is labeled PB TC RX. The PB TC RX signal is output from the CNX board to the LNT board via pin 28 of CNJ-450.

The LNT board serves as "hard wire" connection between the CNX and the CPU. The PB TC RX signal leaves the LNT board at pin 35 of CNJ-441. This signal enters the CPU board at pin 35 of CNJ-421. Once at the CPU board, the PB TC RX signal is buffered and routed to the time code recovery circuit and the Serial Communications Controller (SCC) IC24. The time code recovery circuit is adjusted for optimum duty cycle (as prescribed in Section 6 of this manual). The SCC uses the timing signal developed by the time code recovery circuit to interface the PB TC RX signal to the Z-8002 parallel data bus.

4.2.5.3 CPU Synchronization Operation w/VITC

The Z-8002 will use the data stored in the EPROMs (Erasable Programmable Read Only Memory) to compare the external time code source signal (EXT TC RX) to the playback time code signal (PB TC RX). The Z-8002 will then issue transport servo system control data to the TIB board. This servo system control data will vary depending on the difference between the external time code data value and the playback time code data value. For example, if the time code value difference is over 4 seconds, the CPU will command the transport to enter Shuttle mode to quickly ascend/descend the value of the playback time code value. This will allow a more rapid lock sequence of the playback time code value to the external time code value. When the time code value of the playback data and the external data are relatively close, the CPU simply varies the CAPSTAN REF signal.

4.3 Tape Tension Servo System

The Tape Tension Servo System consists of the following components;

- 1) **Transport Interface Board (TIB)**
Operates as the overall CPU interface to the transport servo and control systems. All transport control/status data is processed through this board. The TIB board is located under the overlay panel between the supply and take-up reel motors.
- 2) **Reel Tach Sensor (RTS) Board X 2 (Supply and Take-up)**
There are two of these boards (one on each of the reel motors) in each APR-5000 Series tape machines. Each RTS board uses a hall effect device to convert the magnetic ring (mounted on the reel motor) flux deviations into TTL pulses. These pulses are used by the CPU to determine reel tape mass radius. The reel radius information is required for proper tape tension calculations by the CPU board.
- 3) **Hall Effect Sensor (HES) Board**
Uses a hall effect device to convert the magnetic flux deviations of the bar magnet (mounted on the tension arm) into an analog (fluctuating DC) voltage. This voltage value is utilized by the CPU to counteract mechanical flutter experienced by the transport during PLAY mode. This process is also termed "Flutter Dampening".
- 4) **Reel Motor Driver (RMD) Board**
The RMD board fulfills the role of the final stage of the reel motor drive circuitry. Two transconductance amplifiers are used to provide drive current for the supply and take-up reel motors. The RMD board is located on the inside of the rear panel (behind the heat sink).
- 5) **Central Processing Unit (CPU) Board**
The CPU board is located under the transport function key panel (on the take-up side of the transport). All functions of the transport (as well as the audio system) are controlled and monitored by the CPU board. The CPU controls and monitors the transport functions and status via the TIB board data bus.
- 6) **Tape Tach Sensor (TTS) Board**
The TTS board is located under the timer roller guide at the immediate left side of the headstack assembly. The TTS board operates in the same way as the RTS board. The two output signals are in quadrature (90-degrees out of phase) and are used by the CPU board for determining absolute tape speed.
- 7) **Reel Motors (2)**

The goal of the Tape Tension Servo System is:

To maintain constant tension throughout the length of the tape regardless of tape position (reel radius) or speed.

To provide the accuracy necessary to fulfill this goal, the APR-5000 utilizes a microprocessor controlled look-up table (ROM table). The CPU board microprocessor communicates with the TIB board via the 16-bit parallel data bus. This data bus provides the control and drive data to the TIB for tension servo control. The TIB (Transport Interface Board) serves as the bi-directional data interface between the CPU and the transport electro-mechanical drivers (on the Reel Motor Driver Board) and the sensors (Reel Tach Sensor Board, Tape Tach Sensor Board, and Hall Effect Sensor Board). As the CPU is to be in control of the transport, it (the CPU) must be aware of the changes in reel motor motion, tension arm position, and absolute tape speed.

This reel motor motion information is provided to the CPU from RTS boards (mounted on each reel motor) via the TIB. The four tach signals (two for each motor) are created as each reel motor rotates. To accomplish this there is a magnetic ring mounted on each reel motor shaft that is polarized alternately North to South. As the poles pass over the hall effect sensors on the RTS boards, a frequency of pulses inversely proportional to the radius of the tape on the reel is created. These pulses are shaped by pulse timing circuits on the TIB board in preparation for reading by the CPU.

The TTS board has two output signals to the CPU board (via the TIB board). To accomplish this there is a magnetic ring mounted on timer roller guide shaft that is polarized alternately North to South. This board also uses a hall effect sensor to detect the changes in flux as the counter roller guide rotates. As the poles pass over the hall effect sensors on the TTS board, a frequency of pulses directly proportional to the absolute speed of the tape is created. These pulses are shaped by pulse timing circuits on the TIB board in preparation for reading by the CPU. The CPU uses this frequency to determine absolute tape speed of the reel servo system.

The HES board also utilizes a hall effect sensor circuit which provides an error voltage to the CPU board (via the TIB board). This analog voltage is converted to a digital data word at the TIB board. This data word is used by the CPU board to minimize the flutter content of the tension servo.

LOCATE BACK TO \emptyset

+ PRESS PLAY 4-20

+ SEE HOW QUICKLY RESPONDS

~ 1/2 sec. to go into play -

The Reel Motor Driver (RMD) provides the drive current for the reel motors as a result of receiving a drive control voltage from the TIB. The RMD board merely operates as an amplifier stage. The RMD does not contain intelligent circuitry for reel motor control. All of the reel motor drive interface circuits are mounted on the TIB board.

The TIB board drives the RMD circuitry upon receiving the appropriate data from the CPU. The TIB converts the 13-bit digital number to the equivalent DC voltage. This DC voltage is combined with the DC voltage interpreted from the TENSION signal. The TENSION signal originates at the HES board.

4.4 Capstan Servo System

The Capstan Servo System consists of the following:

1) Capstan Servo Loop (CSL) Board

The CSL, which is located inside the front panel of the power supply assembly, is a closed phase lock loop system. Capstan motor drive and motor phase stability are the only duties of the CSL. The enable for the CSL and the reference signal originate at the CPU, and are routed through the TIB board.

2) Transport Interface Board (TIB)

Operates as the overall CPU interface to the transport servo and control systems. All transport control/status data is processed through this board. The TIB board is located under the overlay panel between the supply and take-up reel motors.

3) Central Processing Unit (CPU) Board

The CPU board is located under the transport function key panel (on the take-up side of the transport). All functions of the transport (as well as the audio system) are controlled and monitored by the CPU board. The CPU controls and monitors the transport functions and status via the TIB board data bus.

4) Capstan Motor

The CSL ON and CSL A (HI/LO speed select line) commands, along with the CAPSTAN REF (capstan reference signal) originate at the CPU board and are routed through the TIB board to the CSL board. Upon receiving the commands (CSL ON and CSL A) the CSL servo begins comparing the CAPSTAN REF signal (at the phase comparator stage) to the absence of signal on the Capstan Tach lines (upon start-up of the capstan motor there is no signal present), hence the phase comparator will output the maximum error voltage. This large error voltage is routed to the capstan drive stage and is

output to the capstan motor as the start-up signal. As the capstan motor begins to rotate the difference between the CAPSTAN REF and the CAPSTAN TACH signals diminishes to the point of phase lock. At the point of phase lock the LED (DS-1) on the CSL board will extinguish.

4.5 Transport Circuit Descriptions

This section provides a more detailed description of each of the APR-5000 transport circuit boards. By applying the descriptions to follow, along with the schematic diagrams (located in Section 7 of this manual) troubleshooting ability can be improved.

4.5.1 Hall Effect Sensor Board (HES) Overview

The HES provides information on tape tension by monitoring the position of the tension arm. The HES board is mounted to the deck casting directly under the tension arm assembly. Tension arm position is related to tape tension by the mechanical relationship of the arm with the two adjacent roller guides, and the dancer arm spring. A small bar magnet mounted on the tension arm sweeps over the Hall Effect Sensor Chip on the HES Board, which produces a differential output related to the polarity and strength of the magnetic flux. The HES circuits provide differential to single conversion, offset adjustment, and range adjustment to condition the analog output signal for A to D conversion by the TIB.

4.5.2 HES Circuit Description

IC1 is the Hall Effect Sensor itself. The resistors R13 and R14 provide the loads specified by the manufacturer of the HES chip. IC2 and the associated resistors provide differential to single ended conversion and gain. This drives IC2 through RV1 which is the gain adjustment. IC2 inverts the output of IC2 and sums in the offset adjustment provided by RV2. The resistor R12 and Zener diode D1 provide the voltage required by the HES chip. This is approximately 5.1 volts DC.

4.5.3 Reel Tach Sensor Board (RTS-1) Tape Tach Sensor Board (TTS) Overview

The RTS-1 boards (2) are located on each reel motor assembly under the overlay panel. The TTS board is located directly under the timer roller guide on the deck casting. The RTS-1 and TTS are discussed together as they are identical in all respects except for mechanical dimensions of the P.C. boards. The tape tach roller and the reel brake hub assemblies each include a small ferrite ring, which has been magnetized with a sinusoidal magnetic field around its circumference. This field is detected by the DM211 chip, which contains two magneto-resistive sensors (devices which change resistance in the presence of magnetic flux). Three factors: the ring diameter, the number of cycles of magnetic flux recorded on it, and the distance between the two sensors within the DM211 chip are related by design. The result is that, when the DM211 chip is placed near a rotating magnetic ring, its two output waveforms are in quadrature, or 90 degrees out of phase. This is important. These waveforms are amplified and converted to digital signals by circuits on the tach sensor boards. These signals are sent to the TIB for further processing, then to the CPU for measurement. If the CPU were to measure either one of the signals alone, it would be measuring the time required for adjacent zero crossings of magnetic flux to pass by one of the sensors. This method works, but has limited accuracy due to manufacturing tolerances. Instead, the two signals from the tachometer are combined with an "exclusive-or" logic function on the TIB. The resulting waveform represents the time required for one zero crossing of magnetic flux to pass by both sensors. Since the dimensions within the DM211 chip are fixed, the resulting waveform is very accurate and consistent from unit to unit. The direction sense is also derived from the phase relationship of the tach output signals, by using a flip-flop. The left RTS, right RTS, and TTS outputs are processed separately, yielding 3 tach signals and 3 direction signals.

4.5.4 RTS/TTS Circuit Description

IC1, the DM-211 device is the magneto resistive sensor itself. Its power connections are pins 1 and 4. R3, R4 and Zener diode D1 provide approximately 11 volts across the device. The network formed by R5, R6, RV1 and RV2 provides the symmetry adjustment which is covered in the alignment section. This is required due to device to device variations. Pins 2 and 3 of IC1 are the quadrature outputs. They drive directly into IC2 and these stages provide gain and sum in the offset voltages provided by RV1 and RV2.

Notice that there are no input resistors to these amplifier stages as one would normally expect. This is because it is the output impedance of IC1 as seen at pins 2 and 3 which changes under the influence of a magnetic field. Therefore no external input resistor to the amplifier stage is required. The outputs of IC1 pins 2, are sinusoidal waveforms 90-degrees out of phase. These wave forms are applied to IC2 which are connected as zero crossing detectors. Their outputs are square waves of approximately 24 volts peak to peak amplitude. R13 and D3, R14 and D2 clip these waveforms to approximately logic level. These outputs called A and B are sent to the TIB for further processing.

4.5.5 Capstan Servo Loop Board (CSL) Overview

The CSL (located behind the front panel of the power supply unit) is an independent phase locked servo loop for the capstan motor. Its circuits provide signal conditioning for the optical tachometer cells on the motor. It contains the phase comparator, loop filters, and the motor driver. Its power supplies are independently regulated on board, and the control signals from the TIB are optically isolated. This ensures that the CSL is not disturbed by any transients which may be generated by other activity in the tape transport system.

4.5.6 CSL Circuit Description

IC1(1/4, 2/4), IC2, IC3 and IC4, Transistors Q1 and Q2, and their associated components form the tachometer signal conditioning circuits. Each of the tachometer cells A and B have an independent Automatic Gain Control (AGC) loop. These two loops are identical so only one of them will be discussed. The input stage IC1A provides a gain of 20dB for the sinusoidal output of Tach Cell A. This signal can be monitored at TP1 for side A and TP2 for B. The output of the stage is coupled into a passive rectifier and filter. The voltage on the filter corresponds to peak value of the sinusoidal waveform. The second stage, IC1 (4/4) along with transistor Q1, form an inverting integrating current sink. The output of this stage, at the collector of Q1, drives the LED of the tach cell. The LED current through the tachometer cell can be monitored at TP3 for tach cell A and TP4 for tach cell B. These test points have a constant of 1 volt per 10 milliamperes of LED current. The maximum output is approximately 38 milliamperes. The integrators for cells A and B integrate with respect to the same fixed reference, provided by R19 and R20. Since the tach cell output increases along with increasing LED current, this system forms a stable negative feedback loop, such that the peak value of the sinusoidal wave forms at TP1 and TP2 are equal to the reference.

Therefore, both sinusoidal waveforms are the same amplitude. This is important, as these waveforms are combined by IC2 to form the tach sum, which can be monitored at test point 5. For this summing to be accurate, both input wave forms must be of the same amplitude. The waveforms at TP1 and TP2 will nominally be 4 volts peak to peak, and the waveform at TP5 will nominally be 8 volts peak to peak. The output of the tach sum amplifier IC2 is offset to approximately 2.5 volts DC. The tach sum waveform drives the passive filter R24 and C13.

The filtered voltage is applied to the inverting input of the comparator IC3. The tach sum waveform also drives the comparator directly through R25. Therefore, IC3 compares the tach sum waveform against its own DC average. The result is that the output of IC3 is an almost perfect square wave. R26 provides hysteresis or snap action to the comparator. The reason for the 2.5 volt DC offset on the input is that the comparator output is limited from zero to 5 volts DC. Therefore, when this signal is fed back through R26, it provides a symmetrical hysteresis action against the incoming wave form which is centered at 2.5 volts DC. IC4, the 74HC132, is connected as a one-shot which is sensitive to both rising and falling edges of the incoming square wave. Therefore, it outputs a pulse approximately 10 microseconds in duration at both edges of the incoming wave form. The output of this circuit, which is monitored at test point 6 are the tach pulses which are compared against the reference by the phase comparator IC6. IC5 is the optical isolator for the incoming capstan reference pulses. These pulses can be monitored at TP7.

The 74C932 Phase Comparator device provides two outputs. The error pulse at pin 1 is a normally high signal which pulses low for the time duration between the reference and tach pulses, regardless of which came first. In phase lock condition, these pulses are very narrow and do not provide sufficient current to drive the unlock LED DS-1. In an unlocked condition, these pulses at pin 1 become much wider, and sufficient current flows through DS-1 to light it, indicating the unlocked condition.

The Phase Comparator output, pin 5, is a tristate output. If the reference pulse arrives before the tach pulse, the output at pin 5 goes high for the time duration between the two pulses. This drives more current into the capstan motor, making the tach signals "catch-up" to the reference. If the tach pulse arrives before the reference pulse, indicating that the capstan motor is turning too fast, the output at pin 5 goes low for the time duration between the two pulses. This drives less current into the capstan motor, making it slow down. At all other times, the output at pin 5 is a high impedance which does not effect the voltage on the loop filter which follows.

The loop filter has one pole and two zeros which are adjusted by RV1 and RV2. RV1 adjusts the high frequency zero which effects the lock characteristics at low motor speeds. RV2 adjusts the low frequency zero which effects lock characteristics at high motor speeds. This seems backwards, but consider that the kinetic energy stored in the rotating motor increases with the square of the motor speed. Therefore, it takes more high frequency energy to phase lock the motor at low speeds than it does at high speeds.

IC7 is a buffer for the loop filter. Its output can be monitored at TP8. This drives IC7 which is connected as a unity gain differential amplifier. Its function is to offset the loop filter voltage, which is nominally 2.5 volts DC, to near 0 volts DC. This is required because the phase comparator output is limited between 0 and 5 volts DC. As the loop filter voltage deviates from 2.5 volts DC, the phase comparator action becomes non-symmetrical. The motor drive stage, IC8 and the associated transistors form a high gain trans-conductance amplifier. Therefore, as the motor speed is changed from 7.5 to 15 to 30 inches per second, the output of the phase comparator loop filter monitored at TP8 changes very little. Thus the phase comparator operates at near optimum conditions for all motor speeds. This offset stage, IC7, is a major factor contributing to the performance of the CSL over a wide range of motor speeds. IC7 is connected as a band pass filter which compensates the phase lock loop for the characteristics of the motor itself. The output of IC7 can be monitored at TP9 which is the signal driving the output trans-conductance amplifier. JU-2 is not installed in APR-5000 and APR-24 transports. When installed, this jumper allows a CTL error signal generated on the CTL board (of a Sony PCM-3102/3202) to drive the capstan motor directly. In this case, the phase comparator IC6 and the filter circuits which follow it are unused.

The output stage consists of IC8 and the transistors Q3 through Q6. Since IC8 is limited to a maximum of 30 volts across its power supply pins 7 and 4, it is driven from +24 and -5 volts. This is regulated by Zener diodes D8 and D9. This allows the operational amp to drive the output stage over its full range without exceeding the manufacturers specifications for the power supply voltage of the chip. Transistors Q3 and Q4 supply current to increase the speed of the capstan motor. Transistors Q5 and Q6 act to decrease the current through the capstan motor. The motor current flows through R54, a .39 ohm resistor, to ground. The voltage developed across this resistor is fed back to IC8 forming a stable negative feedback loop with a known trans-conductance function.

The capstan motor's life timer is driven by the capstan tach pulses through R57. Therefore the rate at which time accumulates on the timer depends on the speed that the motor is run. The specifications for this time is listed in the O/M manual.

4.5.7 Reel Motor Driver (RMD) Board Overview

The RMD board (located inside the rear panel, behind the heat sink) performs the duty of final stage current driver for the two reel motors. The RMD circuits form two independent trans-conductance amplifiers, one for each motor. These two amplifiers are identical. The RMD receives only three inputs from the TIB. These are the left and right motor voltages corresponding to the desired torque for each motor, and the digital RMD ON command. The nominal transfer function for these amplifiers is 10 volts input for 6 amps output. This transfer function can be trimmed by RV1 for the left motor and RV3 for the right motor. The offset can also be trimmed by RV2 and RV4, so that zero volts input yields zero amps output.

4.5.8 RMD Circuit Description

Since the RMD contains two identical trans-conductance amplifiers, only one of them will be discussed. IC2 (1/2) is a unity gain differential input stage. Its purpose is to compensate for ground shifts between the TIB and the RMD. Its output drives IC3 (4/4) through the gain trim network which consists of R10, RV1 and R11. IC3 (3/4) is the summing amplifier for the output stage feedback loop. The output of IC3 (3/4) drives IC3 (1/4) and IC3 (2/4). These stages, along with Q2 and Q4 are feedback controlled current drivers. IC3 (1/4) and Q2 are active for positive excursions of the input signal. IC3 (2/4) and Q4 are active for negative excursions of the input signal. Q2 provides base current for the output stage pull-up driver Q3.

Q4 provides base current for the output stage pull down driver Q5. Q3 and Q5 each have a capacitor from collector to base to decrease their bandwidth and prevent oscillations. The diodes in the base circuits of Q2 and Q4 serve two purposes. They compensate for the base emitter junction voltage of Q2 and Q4, and provide a dead zone which is intentional crossover distortion. This is required so that the pull up output stage and the pull down output stage never conduct at the same time.

Current through the reel motor flows through R22, a 0.1-ohm resistor to ground. The voltage developed across this resistor is amplified by IC3 (3/4) which is a differential amplifier stage with a gain factor of 10. The motor current may be monitored at test point 1 with a transfer function of one volt per amp. The output of IC3 (3/4) is, in turn, fed back to IC3 (4/4). This closes the feed back loop and provides a stable transfer function.

The trans-conductance amplifier for the right reel motor operates in exactly the same manner, however, note that the left and right reel motor connectors are wired opposite of each other. This was done on purpose. During normal stop or play tension conditions, both motor draw their current from the -24 volt supply. This balances the load on the +24 volt supply, which is the capstan motor and the transport solenoids. During acceleration conditions when maximum current is required, the two motors will draw their currents from opposite supplies depending on the direction of the acceleration. This also acts to balance the load on the power supply.

The RMD ON command is optically isolated through IC1. IC1 drives Q1 which amplifies the signal to drive the relay K1. The relay, when energized, connects +15/-15 volts from the voltage regulators to the operational amps. Turning the RMD on and off in this manner provides a safety feature. If either of the +15 volt or -15 volt regulator were to fail, the operational amps would drive the motors with maximum power, thereby damaging the tape. However, if both the +15 and -15 volt supplies to the operational amps are not present, the output stages do not respond at all. Since the relay coil is driven by the outputs of the voltage regulators, if either of them has failed there will be insufficient voltage to energize the relays and apply power to the operational amps. Only when both the voltage regulators are functioning will there be sufficient voltage to energize the relay.

The fuses, F1 and F2, are provided in case there is some failure on the RMD board. Such a failure will blow the fuses rather than destroying the PC board itself. The diodes D16 and D17 prevent damage to the circuits in case the power supply is connected backwards. This condition will also blow the fuses.

4.5.9 Transport Interface Board (TIB) Overview

The TIB, which is located under the overlay panel between the reel motors, provides most of the interface functions of the tape transport. It performs signal processing of the tachometers, inputs yielding 3 tach signals and 3 direction bits. It performs A to D conversion of the tension analog

signal. It performs D to A conversion to provide the left and right reel motor control signals, a flutter feedback gain control signal, and to drive the vari-speed Variable Frequency Control (VFC). The output of the D/A Converter is multiplexed using a DG212 switching IC. Through this multiplexing one D/A Converter can be utilized for four separate outputs. The TIB decodes the reel motor drive signals (for the RMD), all of the transport solenoid control data and buffers the capstan reference signal.

4.5.10 TIB Circuit Description

IC1 buffers control signals from the CPU. IC2 is an 8 bit bus transceiver for data BITS 0 through 7 to and from the CPU. IC3 is a bus buffer for data BITS 8 through 11 and 15. Both read and write locations and connect to data BITS 0 through 7 on the TIB which requires a transceiver. Only write locations are connected to data BITS 8 through 11 and 15, these require only one way communication. IC4 decodes 5 addresses of locations on the TIB; the A/D Converter read, D/A Converter write, BIT read, BIT write, and SDL write.

IC5 is the sample and hold switch for the A/D Converter which is required to stabilize the input voltage during A/D conversion. It is controlled by 2 bits from IC18; these are tension sample and MVC sample. IC8 (3/4) buffers the sample and hold signal into IC6, the A/D Converter. The CPU reads A/D Converter data by addressing the A/D Converter read location. The A/D Converter BUSY bit, read by the CPU via IC17, prevents the CPU from reading data from the A/D Converter during the conversion period. Each conversion takes approximately 15usec to complete.

IC7 and IC8 (3/4) form a D/A converter. Both the A/D Converter and the D/A Converter use the same reference voltage, provided by the -12 volt regulator, which is trimmed by RV1 and buffered by IC11 (3/4). This A/D Converter and D/A Converter reference voltage is calibrated to precisely -10.24 volts. IC8 (4/4), IC5, and flip-flop IC16 form a phase switching network for the D/A Converter output. Data written to the flip-flop from data bit 15, along with 13 bits of data to the D/A Converter, determine its voltage output. The state of the flip-flop determines whether the analog switch IC15 is on or off, which in turn determines whether IC8 (4/4) is a unity gain buffer or inverter. By convention, the most significant bit of a binary number is reserved for the sign bit, where one means a negative number and 0 is a positive number. Thus the resolution of the D/A Converter is increased to 13 bits, 12 bits of magnitude and one sign bit. The output of the D/A Converter and phase switching network can be monitored at TP4. Notice the binary significance of the A/D Converter - D/A Converter reference -10.24 volts.

See TP4 to -10V

Since the maximum output voltage range at TP4 is -10.24 to +10.24 volts, given 13 bits of data or 8,192 states, each least significant bit change of the data results in 2.5 millivolts of D/A Converter output change. This high resolution is required by the VFC.

*Voltage
Frequency
Converter*

The D/A Converter output drives IC9 and IC10 which form a sample and hold circuit that multiplexes the output of the D/A. This drives the Voltage to Frequency Converter (VFC), the Flutter Dampener (tension arm) Gain (FDG), and Supply/Take-up reel motor signals. IC9 is controlled by 4 sample bits from IC18. The V/F Converter, IC24, is driven by the "VFC" output of the sample and hold circuits and by a constant voltage derived from the A/D Converter - D/A Converter reference. IC11 (1/4) inverts the reference voltage and drives current through RV2 and R16 into the VFC. The sample and hold output at TP5 drives current through RV3 and R17. Pin 1 of the VFC is a virtual ground op-amp input, thus the current flowing through C11 is the net sum of the current from IC11 (1/4) fixed output and IC8 (1/4) variable sample and hold output. This allows the VFC to use almost the entire range of the D/A Converter output voltage; from -10v to +10v. A margin of 0.24 volts remains at each extreme of D/A Converter output to allow for drift of the VFC over time. The VFC output range is 0 to 28.8kHz for -10 to +10 volts input.

The VFC is used to generate the frequency ramp for the capstan motor at start-up, and supplies the capstan reference in vari-speed mode. The Voltage to Frequency Converter output "VARI SRC" is buffered by IC12 (5/6) and sent to the CPU for processing and switching before being used as the capstan reference (only during Vari-speed). The Flutter Dampener Gain "FDG" output of the sample and hold passes through a 20db attenuator before being applied to the control voltage input of IC25, a voltage controlled amplifier. This device determines the gain applied to the AC component of the tension analog voltage, before this signal is summed into the left reel motor output signal. The CPU determines the gain based on the reeling radius of the left reel. This signal passes through a manual gain adjustment network RV4 and IC26 (1/4) which is used to optimize the overall feedback gain to each individual machine.

Sample and hold outputs "LEFT" and "RIGHT" are voltages which correspond to the desired motor torques. The voltages are applied directly to the left and right motor voltage drivers;

IC11 (3/4) and (4/4). The FET transistors Q5 and Q6 are under CPU control, and allow feedback signals to be summed with the motor control voltages when they are on during "PLAY" and "RECORD" modes. IC26 (3/4) drives the gates of Q5 and Q6 under control of the flutter feedback mute bit from IC19.

The resistor/capacitor/diode network at the FET gates provides slow on, fast off, switching action. IC19 also provides "CSL ON", "CSLA", and "RMD ON" commands.

IC20 is an 8 bit latch for solenoid drive commands. Each solenoid has two windings called pull and hold. It is a characteristic of solenoids that much more power is required to pull the solenoid plunger than to hold it in place. Transistors Q1 through Q4 are power MOSFETs which drive the pull winding briefly with approximately one amp of current. IC23 drives the MOSFET gates under control of IC20. IC21 and IC22 provide the hold winding current of approximately 100 milliamperes per solenoid continuously while the solenoid is active. Note that the left and right brake solenoids are driven together by Q4 and IC21. It would be redundant to drive them separately, and the current required is well within the specifications of the driver devices. IC13, IC14, IC15 and IC16 (2/2) are signal processing circuits for the tachometer outputs. IC13 buffers all 6 signals. The exclusive OR gates of IC14 derive the "Left Tach", "Right Tach" and "Tape Tach" signals from the tachometer outputs A and B. IC12 buffers these signals and drives the signal lines to the CPU. IC15 and IC16 derive direction bits from the tachometer outputs which are read by the CPU via IC17. JU-1 is used to access diagnostic and alignment programs designed into the system software. JU-2 is not utilized at this time.

4.5.11 Connector Interface Board (CNX) Overview

The PARALLEL PORT and both SERIAL PORT (TRIBUTARY and BUS CONT EXT) connectors on the rear panel of the APR-5000 are physically mounted on the Connector Interface (CNX) board. The CNX board (mounted on the inside of the rear panel) contains the keyboard matrix encoder, line drivers, and line receivers used for supporting these connectors. In addition, the active combining network and driver circuitry for the CAL IN and OUT connectors is included as well as the input and output amplifier stages used for the LTC TIME CODE IN and LTC TIME CODE OUT connectors.

4.5.11.1 Longitudinal Time Code (LTC) Circuitry

The LTC IN and the LTC OUT connectors (CNJ-454 & CNJ-455) are routed to relays K1 (TC IN) and K2 (TC OUT) which are turned ON whenever the tape machine power supply is ON and the I/O enable (IO EN) signal is active (providing ground to the relays via Q4, Q3). While energized, these connect the time code output from a Differential Line Output hybrid (IC14) or the RS-422 output from IC16. The selection of the output stage is done through the use of the jumpers JU-1, -2, -3, -4. Also during the relay energized state, the LTC input is routed to a TLO74 differential amplifier (IC13). With the machine in the power OFF state, these relays (K1 & K2) connect the LTC IN and LTC OUT connectors to each other forming a "loop-through".

For the LTC output, the time code signal is fed from the CPU board (EXT TC TX) through inverter IC19B. The inverted output is routed to non-inverting input of buffer op-amp IC13A and into the RS-422 driver stage. On the input of the op-amp stage there are two resistor-capacitor networks connected to the drain pins of the FET switches Q4 & Q5 (VN10KM) to ground. The FETs are controlled by the time code equalization (TC EQ-1 and TC EQ-2) signals. These time code output equalization controls originate at the CPU board. They are decoded from the data bus by IC6 (74LS373). IC6 receives an enable for the CPU data to be written to it via the AND function of A8, WR, and CAPSTAN REF by IC2A. The output of the buffer op-amp is connected to the DLO hybrid through RV2 (which is the LTC OUT level adjustment). The DLO also has another trim pot (RV1) used to adjust the output symmetry. The output of the DLO is AC coupled through 22uF capacitors (C20 & C21).

4.5.11.2 Parallel Remote Port

The Parallel Remote Port provides access to the command and status lines of the tape machine.

Electrical isolation for the inputs is provided through opto-isolator couplers. The inputs are active low and connected (through opto-isolators) to the 8279 Programmable Keyboard/Display Matrix Encoder (IC3). As part of the keyboard matrix encoder circuitry, a 74HC138, 3-8 line multiplexer (IC4) is used on the scan line outputs (SL). The outputs of the multiplexer are usually high (+5V) going low when enabled.

The remote manual velocity control (MVC REMOTE) input is different in that it contains the enable command, and the direction/speed of movement. Placing a 1kHz square wave on the input will enable the MVC mode (as will a waveform of less frequency or ground). Varying the duty cycle of the

1kHz square wave will determine the direction and velocity of tape movement. At 50% duty cycle, MVC mode is enabled but no tape movement results. Increasing the HIGH duration (up to 90%) will result in forward movement. Maximum velocity is achieved at 90% duty cycle. Adjustment of the center position for the remote MVC is accomplished through the use of RV3.

Decreasing the HIGH duration results in rewind (reverse movement). Maximum rewind movement is achieved at 10% duty cycle or by grounding the input.

The EXTERNAL Servo Reference Control (EXT SRC) signal also accepts a square wave input. This signal is enabled by another input labelled EXTERNAL Servo Reference Control SELECT (EXT SRC SEL). This signal is used to control the movement of the capstan. When a 19.2kHz signal is injected, standard speed movement will result. This signal, when enabled, will control the capstan reference signal at the CPU board.

4.5.11.3 9-pin Serial Interface Circuitry

Although the serial control interface microprocessor is located on the LNT board, the physical location of the 9-pin connectors is on the CNX board. The circuitry housed on the CNX board is quite basic. The two 9-pin (D-sub) SMPTE/EBU NETWORK connectors (TRIBUTARY PORT and BUS CONTROLLER EXTENSION PORT) enter/exit the CNX board via CNJ-801 & CNJ-802. These connectors are routed to relays K3 (BUS CONT EXT PORT) and K4 (TRIBUTARY PORT) which are turned ON whenever the tape machine power supply is ON and the EXTERNAL I/O ENABLE (EXT I/O EN) signal is active (providing ground to the relays via Q2 & Q3). While energized, these connect the transmit and receive lines of the two connectors to the RS-422 line drivers (26LS31) IC16B, IC16C and receivers (26LS32) IC15A, IC15C. The present software for the APR-5003V utilizes the TRIBUTARY PORT only. Therefore, the active data lines to and from the driver/receiver circuit are Received Data Tributary (RX DA TRIB) and Transmit Data Tributary (TX DA TRIB). These two signals are decoded/encoded at the LNT board. The connection to/from the LNT board is via pins 31 & 32 of CNJ-450.

4.5.11.4 Record/Playback Time Code Circuit

The time code signal to be recorded (REC TC TX) is sent from the CPU board SCC chip via the LNT board. The LNT board simply serves as an interconnect between the CPU and the CNX. The REC TC TX signal enters the CNX board at pin 27 of CNJ-450. From the connector, the signal is routed to pin 1 of IC19A (74HC04 Hex Inverter). The output of the hex inverter is connected to the single-ended to balanced signal converter configuration of IC10C and IC10D. The differential output of this stage leaves the CNX board via pins 1 (Hi) and 2 (Lo) of CNJ-453. This output signal of the CNX board is routed via the interconnect harness to the ADM board connector CNJ-213-3. The ADM board then routes the time code record signal to the TCC board.

The differential playback time code signal is routed to CNJ-453 pins 4 (Hi) and 5 (Lo) by the interconnect harness. The origination point of this harness is at CNJ-213-3 (pins 4 & 5). After entry onto the CNX board, the playback time code signal is directed to the differential to single-ended converter configuration of IC10A and IC10B. The output of IC10B (pin 7) is connected to a line/TTL converter stage (IC11, LM-311). The output of IC11 (pin 7) is TTL buffered and inverted by IC19F. The output of IC19F is labelled PB TC RX and is sent to the CPU board via pin 28 of CNJ-450. The actual signal path of the PB TC RX is through the LNT board. Here again, as with the record time code signal, the LNT board facilitates a simple interconnect function. The LNT board does not have any active components in either the record or playback time code signal path.

4.5.12 Video/Vertical Interval Time Code Translator (VVT) Board

The Video/Vertical Interval Time Code Translator board (VVT) is responsible for video synchronization reference. The main output signal for this board is the Video Synchronization Output (VSR OUT). As explained in Section 4.2.5.1 of this manual, the selection of which port (either the LTC or the Video) is to be used by the APR-5003V as the external reference is made on this board. The main functions of this board are:

- 1) Provide detection and decode capabilities for:
 - VITC
 - Composite Sync (or ref. video signal)
 - Pilot tone (50Hz or 60Hz sinewave or squarewave)

2) Perform actual hardware switching synchronizing between the Video Port and the LTC port.

- LTC Only
- LTC Synchronized to Video Reference
- VITC data Only
- Unique Pseudo time code representation of pilot tone detection

3) Phase Lock to incoming video or pilot tone signal.

In understanding the operation of the board, it is important to first understand the operating modes of the board then a description of the hardware used to accomplish these tasks.

4.5.12.1 Tone Resolve

This mode of operation is useful for internal functions of the machine, and is not specifically designed for external use or recording on the tape. In this mode, the VVT board accepts a 50Hz or 60Hz (such as PILOT tone or monochrome field rate) from which it generates a signal which is similar to time code in format, however the data contained therein would be a fixed value equivalent to a time code value of 31:71:71:13. This will also work with an input frequency of 59.94Hz (color field rate). Relative to the input frequency, the output signal frequency will be one-half, that is, 25 frames/second (EBU), 29.97Hz (SMPTE Drop Frame), or 30 frames/second (SMPTE Non Drop Frame). The output from the VVT is useful for genlocking the internal time code generators of the machine which actually provide time code to the tape and to the LTC OUT connector.

4.5.12.2 Film Resolve

The film resolve mode is similar to the tone resolve mode of operation. In this case the difference will be in the output frequency. Given an input frequency of 60Hz (NTSC monochrome field rate) it will provide an output in the time code format with a frequency of 24 frames/second (FILM time code). The data contained therein will be 31:71:71:31. Note that if the input frequency is 59.94Hz (NTSC color field rate), then the output frequency will be 23.98Hz. As with the tone resolve mode, this output signal is useful for genlocking the internal time code generators which provide time code signals to the heads for recording and to the LTC OUT connector.

4.5.12.3 Video Resolve

In this mode of operation, the VVT accepts a video input from which it will derive a signal which is similar to the time code format. The output of the VVT to the CPU will have a recurring data value of 30:70:70:30. The frame rate of this output will be locked to the frame rate of the incoming video signal. For PAL/SECAM video input, the output frame rate will be 25 frames/second. for NTSC monochrome it will be 30 frames/second and for NTSC color it will be 29.97 frames/second. Again, this signal is internal to the machine and is used for genlocking the internal time code generators which supply signal to the heads (for recording) and to the TIME CODE OUT connector (for output).

4.5.12.4 Video/Film Resolve

This mode of operation is similar to the video resolve mode with a difference in the output frequency. Regardless of the incoming video frame rate, there will be a 5:4 proportional relationship between the incoming frame rate and the outgoing frame rate. For NTSC monochrome signals (or composite digital signals) the incoming frame rate is 30Hz (field rate is 60Hz) which will result in an output signal at the rate of 24 frames/second. The output signal will once again be similar to the time code format with the recurring data of 30:70:70:30. Note that if NTSC color video is fed to the VVT that the output frame rate will be 23.98 frames/second. Again, this signal is internal to the machine and is used for genlocking the internal time code generators which supply signal to the heads (for recording) and to the TIME CODE OUT connector (for output).

4.5.12.5 Vertical Interval Time Code Translate

In this mode of operation, the VVT accepts video signals which contain vertical interval time code signals and translates them to longitudinal time code signals. For PAL/SECAM video signals with EBU VITC, the output will be longitudinal EBU time code signals at a rate of 25 frames/second. For NTSC monochrome video with SMPTE VITC, the output will be longitudinal SMPTE time code at a rate of 30 frames/second. For NTSC color video with SMPTE VITC, the translated output will be SMPTE drop frame LTC at a rate of 29.97 frames/second. The operator is responsible for ensuring that the proper type of vertical interval time code is supplied within the video signal. The VVT will not recognize a mismatch between the video rate and the time code and will translate to the type of time code that should correspond with the frame rate of the incoming video signal. This process will also account for a delay of 1 frame between the incoming VITC and the outgoing LTC. the only

time that this is not a factor is when the incoming VITC is parked (VTR in SEARCH-PAUSE) in which case the data value of the VITC is repeated continuously. Also, in some of the SEARCH or SHUTTLE modes, the some VITC values are omitted from the output and therefore the same result is expected at the LTC output (ascending values). In reverse SEARCH or SHUTTLE operation, the LTC output will be similar with the exception that the values will be descending (note that this is not the same as an audio tape recorder in the rewind direction).

4.5.12.6 Control Signals and Function

Notice that in the hardware configuration that there is no method of determining what type of input signal or what frequency of input signal is being supplied. It is up to the operator to set the internal time code generators to the type of time code which corresponds to the incoming video signal. Also, there are two input signals (MODE A and MODE B) which determine the mode of operation based on the input signal provided.

4.5.12.7 Circuit Description

The inputs to the board can be seen on the upper left side of the schematic (CNJ-400) and on the middle right (CNJ-401). The video input connections come into CNJ-400. This is connected to two jumpers (JU1 and JU2) which select the load resistance for the incoming signal. The first buffer stage is a 5532 op-amp (IC9C) which feeds to the other half of the 5532 which serves as the level clamp. This output routes to a 75207 (IC9B) configured as a high speed comparator serving the function of a Schmitt Trigger or a chopper. The output goes to the SONY CX7913 LSI (IC7C). When valid vertical interval time code is read by IC7C, the DTSE output becomes active driving into a D-flip/flop (74HC74 - IC3CB). The D-flip/flop output drives the VALID VITC LED.

The mode select signals (CNJ401, MODE A and MODE B) connect to 74HC123 one shot (monostable multivibrators) whose outputs go through a NAND gate. These are the control signals which enable one of the two oscillators (Y1- 14.5MHz or Y2-14.318MHz) via the transistors Q1 through Q3.

Also on CNJ401 is the EXT LTC signal input. It is on the VVT that either the external LTC signal or the VVT output is selected. This is done by a 74HC153 multiplexer (IC8AB). The output of the multiplexer becomes the signal labelled VSR OUT which is routed to the CPU external time code receiver input (EXT TC RX).

A 74HC4046 Phase Lock Loop (IC1C) is used for determining whether an unlock condition exists. The error output is connected to a 74HC123 one shot (monostable multivibrator) whose output drives a D-flip/flop (IC5CA - 74HC74). The UNLOCK LED is driven from the D-flip/flop output.

4.5.13 Central Processing Unit (CPU) Board Overview

The CPU board is the system controller for the APR-5000 Series Tape Machines. It communicates directly with the Transport Control Panel (Function Block) KBD assembly for LOCAL commands and status indication. Remote Control input comes from the LNT (originating at the CNX board). Audio system communication is also done via the LNT board. A major upgrade to the assembly has been performed with the inception of the APR-5003V machine and has been incorporated on all APR-5000 Series machines. The newer CPU assembly has a PROM in the IC11 location. The previous assembly (which can not accommodate the SERIAL REMOTE upgrade) utilizes a 74HC138 in the IC11 location.

4.5.13.1 CPU Operating Principles

The transport CPU manages all of the tasks and functions of the tape machine. It addresses, reads and writes data to all portions of the machine. Several major complex functions are carried out on the CPU Board itself. This reduces the external harnessing and bus activity, and provides flexibility in the design. This board is a "Dedicated Process Controller"; a small computer specifically designed to operate an audio tape machine in a modern recording environment.

4.5.13.2 Central Processing Unit (CPU) Circuit Description

IC1 is the Z8002 16-bit CPU chip. All data bus transactions pass through this device. It calculates the addresses of all peripherals. It performs logical and mathematical functions on the data gathered by the peripherals, and commands the performance of the transport interface circuits.

IC2, IC3, IC4 and IC5 perform several functions with most of these gates employed by memory control functions. The logic network formed by these gates activates ROM or RAM (or RWM). It determines if a memory transaction is an even byte, an odd byte, or a word, a read, or a write. IC5 has the additional function of enabling or disabling the read/write memory

entirely. This feature is used during power-up and power-down conditions to protect data stored in the read/write memory. Another separate logic network determines, based on information provided by the CPU chip, when the external data bus will be activated.

4.5.13.3 Programmable Interval Timers (PIT)

IC6 and 7 are programmable counter/timer devices. Each contains five general purpose 16 bit counter/timers which may be programmed individually for many different modes of operation. The Tape Transport System uses these devices for several purposes including tachometer measurements, the CHASE mode, time code synchronization measurements, bias timing, capstan reference switching and dividing, and TVI measurements.

4.5.13.4 RESET Circuits

IC23 generates the system reset. There are three types of resets; the watchdog reset (discussed in previous paragraph), an automatic power-up reset, and a manual reset.

Transistor Q1 is connected so that the +5 volt supply must reach approximately 4 volts before Q1 turns on and begins to charge C4 through R5. When the voltage on C4 reaches the threshold of IC23 (4/4) approximately 0.5 seconds later, the system reset line goes HIGH (+5V) and CPU activity begins. The manual reset is generated by pressing the reset button S1, which discharges C4 and holds the reset line LOW (0V or ground). Releasing S1 allows R5 to charge C4 again, and CPU activity begins as soon as the reset line goes HIGH (+5V).

4.5.13.5 System Clock

Q2 and the associated components are the system clock oscillator at 7.872MHz. Its output is divided by 2 by IC29 to yield the 3.936MHz system clock, with a 50% duty cycle as specified by the manufacturer of Z8000 System devices. This frequency is related by integers to the 19.2kHz fixed capstan reference, SMPTE non-drop frame, and the EBU time code frame rates. Four portions of IC45 are dedicated to driving the signal "PCLK" to all devices on the CPU board which use it.

4.5.13.6 Serial Communications Controller (SCC)

IC24 is a Z8030 Serial Communications Controller (SCC). The CPU programs this device to read and transmit serial time code data. It reads the playback time code and external time code inputs, and outputs record time code and external time code generate. IC26 (1/4) and (4/4) select either the external time code generate or the external time code received signals to be the output time code from the machine.

4.5.13.7 Communications Input/Output (CIO)

IC25 is a Z8036 counter/input/output (CIO) chip. It contains three independent 16-bit programmable counter/timers. Two of these counter/timers generate the 5 millisecond interrupt and the tape tach interrupt. The third counter timer is reserved to generate time code offsets as a backup function. IC26 (2/4) and (3/4) select the appropriate time code clock signal for use with this function.

IC25 outputs several individual control bits including RAM (or RWM), EN, MVC L/R and sync phase reset. It also acts as the system interrupt controller; accepting interrupt requests from the LNT, audio system, keyboard, sync phase measurement circuit, TVI Gate, and the chase function. The Z8030 SCC and Z8036 CIO are the only devices allowed to interrupt CPU activity. When installed the Z8030 (SCC) has the higher priority of the two. The signal "IDC" (Interrupt Daisy Chain).

The IDC signal is output from the Z8030 SCC and acts as an interrupt enable to the Z8036 CIO. The IDC signal is pulled HIGH (+5V) by a resistor when the Z8030 SCC is not installed, as in a two track machine. This gives the Z8036 priority always. Only reset and the NMI signal derived from "PDI" (Power Down Imminent) are higher priority than the Z8030 and Z8036.

4.5.13.8 Time Code Readers

IC28 and IC29 along with IC27 (3/4) and IC32 (1/4) form the sync phase measurement circuits. The inputs are the sync pulses of external and playback time codes. Its outputs are a pulse from IC32 (1/4) related to the time between the two sync pulses. This is measured by one of the counter/timers in IC7. IC27 (3/4) generates "Sync Phase IRQ" when the measurement is complete.

IC30 functions as a "Quantizer" for signals measured by IC6 and IC7. It allows these signals to change only on the falling edge of PCLK, and prevents IC6 and IC7 from generating erroneous numbers.

IC31 through IC37 and IC46 through IC49 are the time code clock recovery circuits. Their inputs are PB TC RX, EXT TC RX and bias ref. Their outputs receive clocks for PB and EXT time code receivers, and transmit clocks for REC and EXT time code generators. There are only four nearly identical circuits used to generate these outputs so only one will be discussed in detail.

IC31 and IC32 (3/4) and (4/4) generate narrow LOW (0V or ground) pulses on each transition of the input time code signals. These pulses trigger the receive clock recovery circuits for PB and EXT time code. IC33 and 35 (4/4) and the associated components form a frequency to voltage converter.

The output of IC35 (4/4) resets at +2.25 volts DC, given no time code input, due to the offset provided by R37 and R38. This offset is required by the specifications of the manufacturer of the RC4152 devices. The output of IC35 (4/4) goes increasingly negative with increasing bit rate of the incoming time code. IC37 is connected as a voltage controlled one shot (voltage controlled monostable multivibrator). It is triggered by the transition pulses from the time code input, and controlled by the output voltage of IC35(4/4). Its time constant is adjusted by RV1 to be nominally three fourths of a bit cell time. Its output at pin 3, monitored at test point TP9, goes LOW (0V or ground) when triggered at pin 6, and it cannot be re-triggered until its time constant is complete. The time code transition pulses at one-half bit cell intervals caused by encoded ones in the time code data, will not trigger the device. Only transition pulses at bit cell boundaries will trigger IC37. Thus the falling edge of the receive clock waveform occurs shortly following each bit cell boundary (due to propagation delays of the circuits), and the rising edge occurs at approximately three fourths of a bit cell time. The Z8030 SCC uses this waveform to identify encoded ones and zeros in the serial time code and decode the time code data. The FVC output of IC35 (4/4) causes the time constant of IC37 to become shorter along with increasing time code bit rate, therefore the recovered time code clock waveform tracks changes in the bit rate of the time code. It automatically adjusts for DF, NDF, and EBU time code, and tracks changes of bit rate caused by VARI-SPEED operation and synchronization.

4.5.13.9 Time Code Generators

The record transmit clock circuit works in the same manner as the external receive clock circuit, but it is triggered by the falling edges (bit cell boundaries) of the EXT RX CLK circuit instead of the transitions of the input time code. This circuit is used to provide the REC TX CLK waveform, monitored at test point TP8, which has rising edges at bit

cell boundaries and falling edges at one-half bit cell intervals. This waveform allows the Z8030 SCC transmitter to encode the time code data, provided by the CPU, into the bi-phase mark (FM1) serial time code data format with a correct wave shape.

The time code recovery circuits are found on the standard cards of the APR-5000 Series machines, but they are unused. Only the APR-5003/5003V Series machines have the additional hardware required to utilize the functions of these circuits.

4.5.13.10 Principles of Operation, TC Clock Recovery

This circuit enables the APR-5003/5003V to recover and decode the time code signals. This circuit is used in both the PB, and REC modes of the machine. All offset and PB, SYNC, REC functions are enabled by the user and are under software control.

4.5.13.11 Circuit Overview

The basis of the time code Control is performed by the 8030 (IC24) on the CPU Board. The CPU programs this device to read and transmit serial time code data. This device reads the Playback, time code and External time code Input and Outputs, the Record time code, and supports the External time code generator.

The frequency determining device is the System Clock whose integers of frequencies relate to the 129kHz fixed capstan reference, SMPTE (non-drop frame), and EBU time code fixed rates.

SMPTE Drop frame is generated by control of software and the installation of IC21 a TCXO (Temperature Controlled Crystal Oscillator). IC26 selects the internal or external time code source.

IC31 through IC37 and IC46 through IC49 are the time code clock recovery circuits. Their inputs are PB TC RX, EXT TC RX, and bias reference. Their outputs are receive clocks for PB and EXT time code receivers, and transmit clocks for REC and EXT time code generators. There are four nearly identical circuits used to generate these outputs so only one will be discussed in detail.

IC31 and IC32 (3/4) and (4/4) generate narrow low pulses on each transition of the input time code signals. These pulses trigger the receive clock recovery circuits for PB and EXT time code. IC33 and IC35 (4/4) and the associated components form a frequency to voltage converter. The output of IC35B rests at +2.25 volts DC, given no time code input, due to the

offset provided by R37 and R38. This offset is required by the specifications of the manufacturer of the RC4152 devices. The output of IC35D goes increasingly negative with increasing bit rate of the incoming time code.

IC37 is connected as a voltage controlled one shot. It is triggered by the transition pulses from the time code input, and controlled by the output voltage of IC35B. The time constant is adjusted by RV1 to be nominally three-fourths of a bit cell period. The output at pin 3, monitored at test point 9, goes low when triggered at pin 6, and it cannot be re-triggered until the time-out (determined by the time constant) is complete. The time code transition pulses at one-half bit cell intervals, caused by encoded ones in the time code data, will not trigger the device. Only transition pulses at bit cell boundaries will trigger IC37. Thus the falling edge of the receive clock waveform occurs shortly following each bit cell boundary (due to propagation delays of the circuits), and the rising edge occurs at approximately three fourths of a bit cell time. The Z8030 SCC uses this waveform to identify encoded ones and zeros in the serial time code and decode the time code data. The F/VC output of IC35D causes the time constant of IC37 to become shorter along with increasing time code bit rate of the time code. It automatically adjusts for DF, NDF, and EBU time code, and rates changes of bit rate caused by vari-speed operation and synchronization.

The record transmit clock circuit works in the same manner as the external receive clock circuit, but it is triggered by the falling edges (bit cell boundaries) of the EXT RX CLK circuit instead of the transitions of the input time code. Its function is to provide the REC TX CLK waveform, monitored at test point 8, which has rising edges at bit cell boundaries and falling edges at one-half bit cell intervals. This waveform allows the Z8030 SCC transmitter to encode the time code data, provided by the CPU, into the bi-phase mark (FMI) serial time code data format with a correct wave shape. The fact that the cell boundaries are marked by falling edges of the receive clocks and rising edges of the transmit clocks is simply a function of the design of the Z8030 SCC chip itself, and is the reason that IC8A and C connected as inverters are required.

The circuits formed by IC34 through 48 are identical to those just described. It accepts playback time code as an input, monitored at test point 4, and develops PB RX CLK and EXT TX CLK as outputs, monitored at test point 10 and test point 7 respectively.

4.5.14 Local/Network Transceiver (LNT) Board Overview

Since the Local/Network Transceiver (LNT) board is a multiple function PC Assembly mounted inside the rear panel of the tape machine, communications between the CPU and the CNX are routed through the LNT as well as communications between the CPU and the audio system. To facilitate explanation, the circuits are divided into functional blocks.

4.5.14.1 Central Processing Unit (CPU) Block

IC21 (8085) is the processor that controls all functions within the LNT. Address lines A8 through A15 address the memory ICs, IC13 (ROM) and the scratch pad memory of IC6 (RAM). In addition IC3 is an address decoder for the 8085. Address A0-A7 addresses the SCC/Serial Communications IC25 (8530).

4.5.14.2 Serial Communications Controller (SCC) Block

The Serial Communications Controller (IC25 - 8530) handles serial protocol data at a Baud Rate of 38.4 Baud. The SCC determines the type of serial protocol according to the setting of DIP switch S1.

The output of S1 is buffered by IC2 (74LS244) and uses address lines A0-A7 to carry the information. However, IC2 can only be enabled when pins 1 and 19 are active LOW (0V or ground), so during this time the 74LS244 outputs are active and the DIP switch can be read.

This signal is transmitted from pin 14 of the decoder IC9 (74LS138). The 74LS138 outputs are HIGH unless enabled. This chip select signal is qualified by the SCC interrupt (output of the 8530) to determine whether the SCC or the FIFO is activated. The SCC will issue interrupt to 8085 CPU when the data receiving port or the transmission port are ready.

The transmission (TX) data will be switched between the TX of this SCC and the TX of the other tributary of lower chain, in order to perform the multiple time shared bus. This switch is controlled by RTSB which is used as a general purpose output.

4.5.14.3 Random Access Memory (RAM) Interface Block (FIFO RAM)

IC19, IC20, IC23, and IC24 are working as a "First-In First-Out" (FIFO) RAM block. Since both the CPU Processor and the LNT Processor run on independent clocks, the FIFO is required to prevent overload to the input buffers of the Transport CPU board.

These signals are timed by a gating network consisting of IC1, IC5, IC8, IC15, and IC16. The command structure for the handshake sequence is as follows:

LNT to CPU

1. LNT has data to be sent
2. LNT loads data to FIFO
3. LNT issues int. to Z8000
4. Z8000 unloads data from the FIFO
5. LNT can know that data is ready by Z8000 by watching "busy" signal.

CPU to LNT

1. Z8000 has data to be sent
2. Z8000 loads data to FIFO
3. Z8000 issues INT to LNT
4. LNT unloads data from the FIFO
5. Z8000 can know that data is ready by LNT by watching "BUSY".

4.5.14.4 Audio System Data Block

In addition to the data sent between the LNT and the CPU, the LNT also has control between the audio system (MST card) and the Transport CPU board. IC10, IC18, and IC22 provide a path for which this data can flow.

IC10 is a uni-directional device that sends the latched addresses (LA) to the Audio System. These are used by the CPU to determine the parameters of the audio system to be enabled.

IC18 and IC22 are bi-directional devices that send and receive the data to and from the Transport CPU. These buffers are inactive until the AUDIO IRQ is active.

The two communication lines, the serial communication port and the audio system data transfer are time-shared. The timing sequences are based on two independent interrupt lines; the LNT IRQ (serial communications port) and the AUDIO IRQ (audio system).

4.5.14.5 Explanation of Signals

The various input and output signals of the LNT board are explained with the pin-out charts in Tables 4-1, 4-2 and 4-3.

NAME	TO	FROM	EXPLANATIONS
BCSB	X		BUFFERED CHIP SELECT
BIAS REF.	X		BIAS REFERENCE FOR APR AUDIO SYSTEM
RESET	X		SEE CNJ440
BIAS PULSE	X		BIAS PULSE FOR APR AUDIO SYSTEM
ACALINT		X	INTERRUPT FROM APR AUDIO SYSTEM
WR	X		WR OF Z8000
ACNTLINT		X	INTERRUPT FROM APR AUDIO SYSTEM
RD	X		RD OF Z8000
A15 DA0	X	X	Z8000 DATA BUS
AA8 AA11	X		BUFFERED Z8000 ADDRESS

Table 4-1. CNJ442 TO/FROM AUDIO SYSTEM

NAME	TO	FROM	EXPLANATIONS
DO -> D15	X	X	Z8000 CPU Bus
MONITOR CS	X		CHIP SELECT
RDZ	X		Z8000 RD (Buffered Read Enable)
WRZ	X		Z8000 WE (Buffered Write Enable)
RESET	X		SOFTWARE PROGRAMED RESET
A8	X		Z8000 A8
BIAS REF.	X		BIAS REF SIGNAL FROM CPU
EXT SRC		X	EXT CAPSTAN REFERENCE (PARALLEL REMOTE)
TAPE TACH	X		ROLLER PULSE TO OUTSIDE
TAPE DIR	X		TAPE DIRECTION TO OUTSIDE
REMOTE CS	X		CHIP SELECT
MVC ANALOG		X	MVC CONTROL SIGNAL (DC Voltage)
REC TC TX	X		GENERATOR TC TO BE RECORDED (Internal Generator)
PB TC RX		X	REPRODUCED TC FROM TAPE (Internal Reader)
EXT TC RX		X	TC FROM REAR PANEL (External Reader)
EXT OUT TC TX	X		GENERATOR TC TO OUTSIDE (External Generator)

Table 4-2. CNJ440 TO/FROM CNX

NAME	TO	FROM	EXPLANATIONS
MVC ANALOG	X		SEE CNJ440 EXPLANATION
DS		X	Z8000 DS
R/W		X	Z8000 R/W
LA8 -> LA11		X	Z8000 LATCHED ADDRESS
D0 -> D15	X	X	Z8000 DATA BUS
BIAS REF		X	BIAS REFERENCE
EXT SRC	X		SEE CNJ440 EXPLANATION
TAPE TACH		X	SEE CNJ440 EXPLANATION
BIAS PULSE		X	BIAS PULSE FOR APR-AUDIO SYSTEM
AUDIO CS		X	CHIP SELECT
AUDIO IRQ	X		INTERRUPT REQUEST FROM AUDIO SYSTEM
LNT CS		X	CHIP SELECT
LNT IRQ	X		INTERRUPT REQUEST FROM LNT
REC TC TX		X	SEE CNJ440 EXPLANATION
PB TC RX	X		SEE CNJ440 EXPLANATION
EXT OUT TC TX		X	SEE CNJ440 EXPLANATION
EXT IN TC RX	X		SEE CNJ440 EXPLANATION
CAPS REF		X	SEE CNJ440 EXPLANATION
EXT TACH	X		SEE CNJ440 EXP.

Table 4-3. CNJ441 TO/FROM CPU

4.5.15 Key Matrix Board (KBD)

The KBD board is located under the key panel of the APR-5000 Series tape machine. Basically, it consists of the control circuitry which forms the keyboard/display matrix arrays for the front panel switches and indicators. Included are the data bus drivers and the fluorescent display driver. The End Of Tape (EOT) sensor circuit is also located on the KBD board. The KBD board serves as the local user interface to the CPU system.

4.5.15.1 8279 Programmable Keyboard/Display Interface Block

The heart of the KBD board is the 8279 Programmable Keyboard/Display Matrix Encoder. This is a Z8000/8085 microprocessor peripheral device used for creating the keyboard and display matrix arrays. It communicates with the microprocessor directly via the 8-bit parallel data bus.

The 8279 is programed at initialization or reset of the CPU. It creates two matrix arrays using multiplexer and buffers for support. The display matrix includes the LED indicator LEDs on the front panel of the machine and the fluorescent display drivers which drive the TAPE TIME and LOCATE TIME

displays on the DSP board. Lamps in the transport control switches are also part of the display matrix array via FET control switches on the KBD board. A 74HC138 (3 to 8 line decoder) is utilized in the display matrix array. Using this configuration, a more expansive array can be realized.

The keyboard matrix array consists of the top panel keys and switches on the APR-5000. Multiplexing is performed using a 74HC138 3 to 8 line decoder.

4.5.15.2 Latched Address Decoding

Various control signals and address lines are routed to the KBD board. These are buffered using a 74HC245 bi-directional bus transceiver IC1. IC1 is configured such that it will only receive signals from the CPU board. The outputs of IC1 are normally HIGH (+5V) unless enabled. These are the active LOW chip select signals used for enabling the various portions of the KBD board.

4.5.15.3 End-Of-Tape (EOT) Sensor Circuit

The EOT sensor circuitry is also found on the KBD board. This consists of the adjustable op-amp comparator circuits (for sensor) and the LED driver circuit (Q9). The comparators are fed from the photo-transistor in the EOT assembly via pin 3 of CNJ-443. Adjustment of the EOT sensitivity is performed by the potentiometers RV3 & RV4. Two circuits are included so that each may be set to a different sensitivity (for instance, one for sensing leader tape and the other for sensing the presence of recording tape). Most applications require the use of RV4 as the adjustment. The output of this circuit is returned to the 8279 via RL1 (Return Line 1). The 8279 encodes the data for output to the CPU.

**** NOTE: If the CPU does not receive this data from the KBD, all transport functions are disabled.**

4.5.15.4 MVC Touch Sensor Circuit

The Manual Velocity Control (MVC) wheel on the top panel of the APR-5000 is made of metal and is directly connected (via the PC board trace) to R63. R63 is the input resistor for the MVC touch sensor circuit configuration of IC22 (2/2) and IC8 (LM-311). The capacitance of the human body will be sensed at the input of IC22, this causes a toggle of the

output which is connected to the input of IC8. IC8 is used as a line level/TTL converter. The output of the converter is routed to the 8279. The 8279 performs the encoding process on the data received and outputs this data to the CPU. Upon receipt of this data, the CPU issues the appropriate data to the TIB board for manual transport velocity control and illuminates the MVC LED (DS-4) on the KBD board.

SECTION 5 AUDIO CIRCUIT DESCRIPTIONS

5.0 Overview

This section provides the required information for understanding and troubleshooting the audio system circuitry of the APR-5000. By following this narration through the block diagram description into the detailed circuit theory, the technician will be able to grasp the operation and signal flow of the audio system.

5.1 Audio System Signal Flow

Refer to Figure 5-1 ChaNneL (CNL) Card Block Diagram (page 5-3) and Figure 5-2 Audio System Interconnect Block Diagram for this tutorial. There are two basic signal flows to cover, one is the RECORD signal flow and the other is the PLAYBACK (SYNC or REPRO) signal flow. As the origination of the two signal flow paths differ, they will be covered separately.

5.1.1 Record Signal Flow

Upon entering the machine via the AUDIO INPUT connectors, the differential signal is routed to the AuDio Mother (ADM) board by way of a shielded cable harness. Upon reaching the ADM the input signal is routed from the connector CNJ212-N (N being the corresponding channel number) to the appropriate ChaNnel/Time Code (CNL/TCC) Card edge connector CNJ211-N (N being the corresponding channel number) pin 1 (HOT) and pin 2 (COLD). The first stage of the CNL/TCC card that the RECORD signal is presented to is the Differential Line Input Hybrid. This stage unbalances the input signal and buffers the CNL/TCC circuit from external circuitry. The signal is then routed to the digital switch (DG212) which controls the signal routing for the RECORD circuitry and the LINE OUTPUT circuitry. For example, in RECORD mode the input signal will be sent to the RECORD circuit for recording onto the tape, but remember that the LINE OUTPUT signal is selected by the control keys on the remote control unit, hence in RECORD mode the LINE OUTPUT signal can be either the REPRO signal (from the Reproduce head) or the INPUT signal (from the LINE INPUT connectors).

In the RECORD mode the signal to be recorded is directed to the Record Level Digitally Controlled Resistor (DCR). This section of the CNL/TCC card controls the amplitude of the signal level to be recorded and the Record EQ by reading the 8-bit data from the CPU board. A buffer stage separates these two stages. The Record Secondary Feed Forward and Record Secondary Feedback are separated by a buffer stage and control the Record signal compensation. These compensation functions are performed by simple switching networks that enter different combinations of capacitors into the filter network. The selection of what combination is used is determined by the audio data from the CPU. The eight control data bits are divided into two, four bit data lines. The upper four bits are used for Feed Forward, and the lower four bits are used for Feedback control. The output of this section of the CNL/TCC card is the Record Drive signal. The Record Drive signal exits the CNL/TCC card (via connector CNJ211-N pin 8A) to the ADM board, where the signal is routed to the Front End Transformer (FEX) board via pin 6 of CNJ213-N. The FEX board is the point of combination for the Record Drive signal and the Bias signal. It is here (at the FEX board) that the final relay switch is thrown, thus connecting the entire Record circuit from the LINE INPUT connectors to the RECORD/SYNCHRONOUS PB head.

The Bias and Erase signals originate on the Master (MST) card. These signals (Bias and Erase) are routed from the MST card (as clock signals) to the CNL/TCC cards via the ADM board. The Bias and Erase clock signals enter the CNL/TCC card(s) at CNJ211-N pins 33A (Bias) and 33B (Erase). These signals are processed through the Ramp Generator where the timing for Ramp Up and Ramp Down is determined. The Bias and Erase signals are then sent to a current multiplier stage. The current multiplier stage houses the ON-BOARD adjustment of the Bias and Erase signals. A digital switch controls the output of the current multiplier, thus controlling the input of the next stage, the final Erase and Bias drive circuits. The Bias and Erase driver circuits amplify the signal to the final level for the Bias and Erase heads. Both the Bias and Erase signals are output from the CNL/TCC card and routed to the FEX board via the ADM and the shielded cable. Upon arrival at the FEX board, the Bias signal is combined with the Record Drive signal and directed to the RECORD/SYNC head. The Erase signal is routed to the 1:10 step-up transformer. The output of the transformer is directed to the ERASE head.

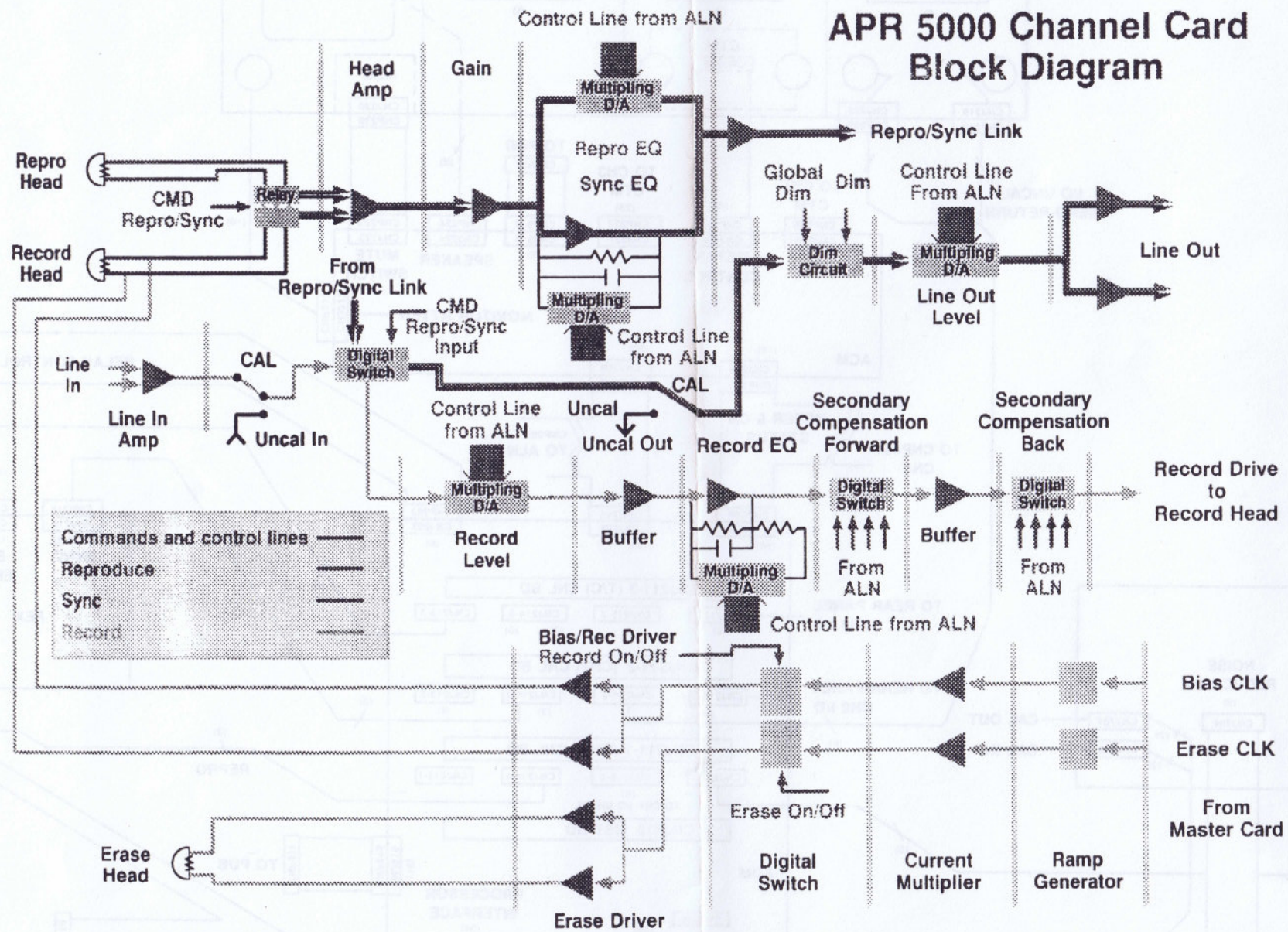


Figure 5-1. APR-5000 CNL Block Diagram

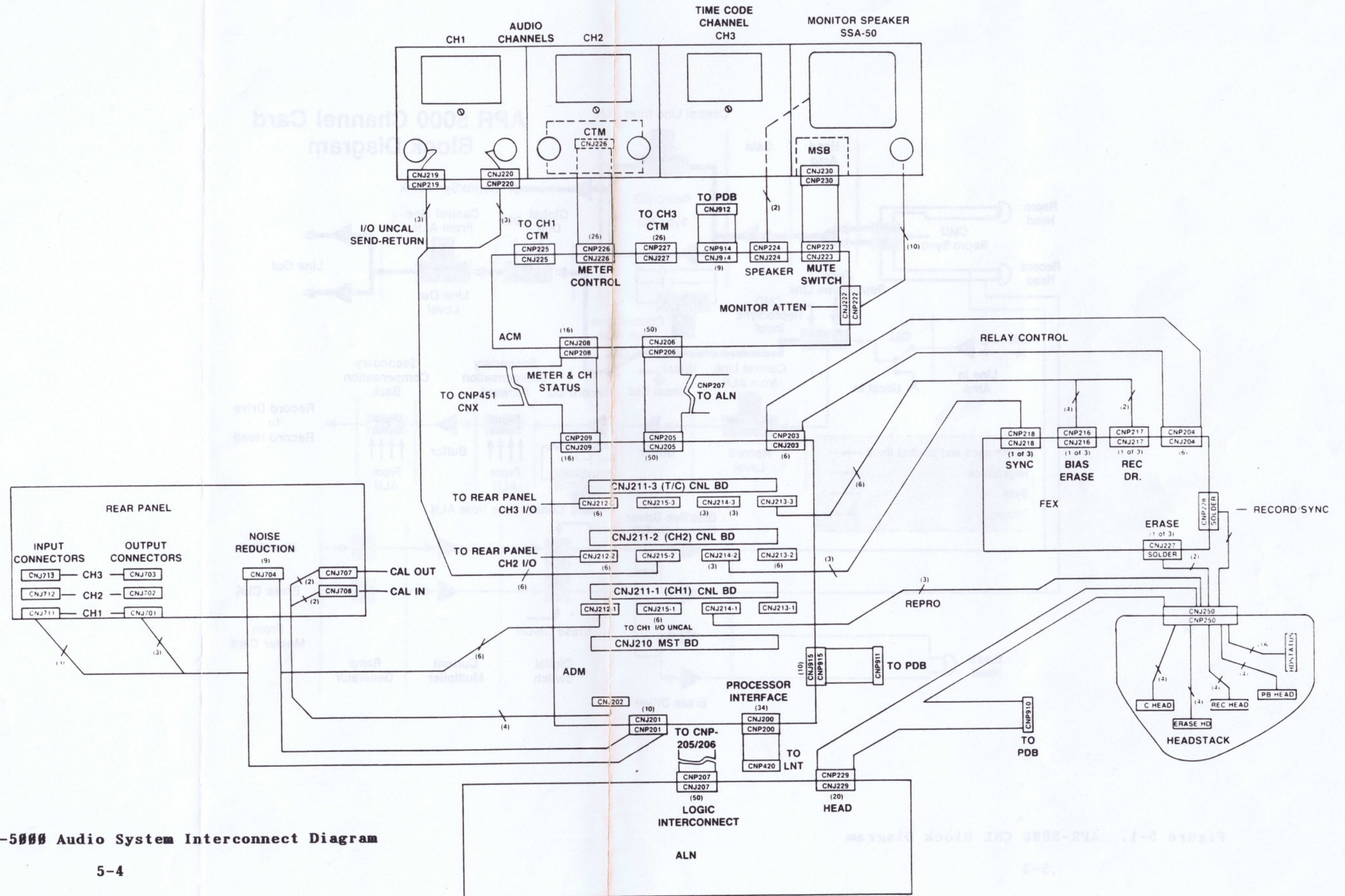


Figure 5-2. APR-5000 Audio System Interconnect Diagram

5.1.2 Playback Signal Flow

For playback of the recorded signal, there are two heads that are capable of performing this function. They are the SYNC and REPRO heads. The selection of the source head is made by the operator by pressing the desired mode switch on the remote control unit (refer to Section 3 for operation instructions). This keystroke is received by the processor, where it becomes part of the audio system data stream. This audio system control data stream (8-bit parallel) is received at the CNL/TCC card where it is decoded into the discrete control lines for control of the audio switching and commands necessary on the CNL/TCC card. Once the selection of the playback head (either REPRO or SYNC) is made, the Head Amplifier stage of the CNL/TCC card will receive the appropriate playback signal. The Head Amplifier stage and proceeding EQ Buffer stage both provide the necessary gain to the signal for processing through the EQ circuitry. After the signal is amplified, it is directed to the EQ stage. The EQ stage consists of a multiplying D/A which is controlled by the 8-bit data from the ALN Panel. The EQ stage performs both high and low frequency equalization of the playback signal. This post EQ signal is routed to the Head Gap Compensator (HGC) circuit. The HGC circuit compensates for variances in head gap spacing (it is common to experience small differences in head gap from head to head). The output of the HGC circuit is labeled REPRO/SYNC LINK, and is directed to the digital switch (which controls the input to the LINE OUT circuit). The command for the switch to pass the REPRO or SYNC signal instead of the INPUT signal is a combination of two command lines, the REPRO/SYNC command and the INPUT command. When either REPRO or SYNC is selected, the playback signal is routed from this digital switch to the DIM circuit. The DIM circuit provides control of the LINE OUT signal by the ALN circuitry. This control allows the LINE OUT signal to either pass at full level or be defeated by the manipulation of the ALN control keys. The final stage in the playback signal path is the LINE OUT Amplifier. This stage provides the final amplification to line level and balancing of the signal. From the LINE OUT amplifier the signal is routed to the rear panel output XLR connectors via two conductor shielded cable.

5.2 Audio Circuit Descriptions

As an aid in troubleshooting the audio circuitry of the APR-5000, the following sections detail the operation of the individual cards. To gain a better understanding of the audio system of the APR-5000, it is recommended to precede this section by reading the block diagram explanation in Section 5.1. In studying this section, refer to the schematics provided in Section 7 of this manual.

5.2.1 Master Card (MST) Overview

The Master Card provides all common requirements of the audio channel cards. All CPU interface circuitry, Master Bias and Erase signals and Record Ramp signals are incorporated into the MST card. The MST is located at the bottom of the audio card section (under the transport casting). Additionally, the MST card provides the interface to the rest of the audio system which encompasses the Alignment Panel (ALN) and audio monitor control functions in the Remote Control Unit.

The tasks performed by the MST card include the following:

- 1) Audio Address Bus Interface (DWR-0 through 3, CHAN-0 through 7, PA-0 through 7)
- 2) Record Hold Command Generation
- 3) Erase Stagger Delay Generation (ERASE PULSE O, ERASE PULSE E)
- 4) Erase and Bias Ramp Rate Generation (ERASE CLK, BIAS CLK)
- 5) Erase and Bias Signal (sine wave) Generation
- 6) CAL SUM ACN Buffer
- 7) CPU Audio Data Bus (from the LNT board) Loop-through

Interfacing of this board with the audio system control keys on the Remote Control Panel is performed by the Connector Interface (CNX) board.

5.2.2 MST Circuit Description

The data provided to the MST is in 8 bit parallel format (ADTA-0 through ADTA-7). One half of the bits provide data directly. There is also an 8 bit parallel audio address bus input to the MST card which provides the addressing to the 3 eproms of the Master Card. This address information is routed to the eproms IC22, IC23 and IC24. These devices are not being used in their conventional fashion but as pre-programmed device selects, determining the parameters PA-0 through PA-9, channel selects (1 through 3). The multitrack audio drawer selects (1 through 3) are used on the APR-24 Series. The APR-5000 Series will enable only one drawer command, since there is only one drawer. Drawer 0 performs routing program maintenance within the MST card. IC25C and IC13B are ROM Chip Select (CS) devices, when the BCSB line goes low. The data portion of the 16 bits is directed from the data buffer IC27 to IC28, IC29 and IC30. IC28 provides the REC HOLD and REC HOLD commands, ERS PULS and ERS PULS clocks, and the ESD-0 through ESD-3 data (Erase Stagger Delay data).

The REC HOLD and REC HOLD commands are utilized for the global REC HOLD command. The REC HOLD and REC HOLD commands are routed to IC14B and IC14C, which are used as a conditioning circuit for the final REC HOLD Command Driver (Q1 and Q2). The ERS PULS and ERS PULS clocks are directed to IC14A and IC14D for pulse timing. The output of IC14A is routed to IC15, which creates the erase pulses (ERASE PULSE O) for the odd channels (1, and 3). The Q2 output of IC15 is also connected to the input of the ERASE STAGGER DELAY circuit (IC16 and IC17). This connection allows the synchronization of the odd and even channel erase pulses. The erase stagger delay data (ESD-0 through ESD-3) output from IC28 is used to manipulate the timing of the ERASE PULSE E (even channel erase pulse) signal. The Delay count is clocked by a 2400 Hz signal which has been derived from the CPU 800 kHz clock reference (IC5, IC6). This clock frequency of 2400 Hz is divided to clock the bias and erase ramp rate bits. For detail into the timing of the delay, refer to the chart on the MST board schematic diagram in Section 7 of this manual. These Erase delays are used to compensate for odd and even channels in heads that have staggered erase head architecture. IC29 is used to provide Erase ramp control and Bias ramp control data to IC18 (ERASE RAMP RATE GENERATOR) and IC19 (BIAS RAMP RATE GENERATOR). The ERASE RAMP RATE and the BIAS RAMP RATES are not adjustable by the user on the APR-5000 Series machines.

IC30 provides global dim control of all channel cards when in Stop or Fast Wind modes. (This dim can be defeated in Fast Wind mode by enabling lifter defeat.) In addition, IC30 provides headstack poll integration to confirm that the head stack is properly programmed for a designated machine. Individual parameters select for all 3 ICs (IC28, IC29, and IC30) is accomplished using IC26. This provides the selection of PA (Parameter Address) enables (PA-0 through PA-2) and allows the enable and capture of data from the data bus when the WRBS line goes low.

IC3, and IC4 divide the 798.72kHz reference signal (from the CPU) to derive the 400kHz and 100kHz bias and erase clocks respectively. The output of IC3 is connected to a tuned filter network of IC7, and IC8. The circuit of IC9 creates the final stage buffer amplifier providing the gain to drive a maximum of 8 channels of erase circuitry. The transfer function of this circuit provides a clean sinusoidal output of the 100kHz Erase signal to the CNL/TCC cards of drawer 1. The output of IC4 is also connected to the same type of square wave to sine wave convertor network for shaping of the 400kHz Bias waveform. The MST provides an additional feature when doing audio alignment. Calibration input and output audio feeds (slate and cal sum) are provided by IC2. These connections appear on the rear of the machine on BNC Connectors. A calibration sum amplifier allows the routing of signals to all channels.

IC1A is an ACN (Active Combining Network) buffer amplifier similar to the circuit used in audio consoles. This provides a weighted sum of all signals. When any number of channel signals are selected via the ALN panel, these channels combine with no increase of signal level. This signal is output to the Audio Signal Board (ASB) located in the meter bridge housing where the VU meter provides the metering for the CAL SUM BUS.

On board regulation is provided by two 3 terminal Monolithic type regulators (IC20 - IC21). The input to these regulators is a regulated +/- 18 volts. These regulators are provided to isolate the MST Card from digital influence within the system. This regulation circuit has the flexibility of being configured as either a fixed regulator circuit, or as a variable regulator circuit (refer to the schematic diagram in Section 7 of this manual).

5.2.3 Channel Card (CNL) Overview

The Channel Card (CNL) incorporates all of the audio signal record/reproduce circuitry and performs all audio signal processing within its respective channel of the APR-5000 audio system. The CNL is controlled by two data busses, the Audio Data Bus (ADTA-0 through 7 from the CPU board) and the Parameter Address Bus (PA-1 through 9 from the MST Card). The Audio Data Bus provides the CNL with all keystroke and program information that is sent from the CPU. Control of all CNL cards is performed by the MST card. The Master Card converts the Audio Address Bus (AADR) from the CPU into the Parameter Address Buss (PA-0 through 9). The Audio Address Buss is an 8 bit buss that controls a precoded set of parameter enables, channel enables, and drawer enables. The pre-encoded parameter enables allow latching of selected data to the appropriate latches on the CNL card. In addition, this data is also directed to the Digitally Controlled Resistors (DCR) which are the amplitude varying devices within the alignment circuitry.

5.2.4 CNL Circuit Description

The Audio Data Buss (ADTA-0 through 7) is connected to the inputs of IC28 via the edge connector pins 36 through 39 A and B. This device is a data buffer. The data is latched by the array of latches and Digitally Controlled Resistors (DCR) when the WRBS pulse is in an active low true state. Additionally, the Parameter Address bits (PA-1 through 9) are decoded by IC32 into the following dedicated commands:

- 1) Monitor Calibration
- 2) Monitor Bias
- 3) Repro Equalization
- 4) Record Equalization
- 5) Secondary Compensation
- 6) Gap Compensation

These dedicated command lines share a common enable. When the CHAN N command and the DRAWER N command are decoded by the OR gate of IC34A with a resultant low logic state, the parameter command lines are activated. IC29 latches the data for Secondary Gap Compensation control, input and output uncalibration level, Record Enable, Dim Inhibit and other frequency related switching functions (LEM Defeat, etc.).

IC30 latches the mode functions that allow the control of Repro/Sync routing to the reproduce circuitry, DIM circuit, calibration input switching, and individual Record/Sync switching. IC31 provides the latching of data for Secondary Record Compensations as well as Bias and Erase Ramp timing. This is accomplished by the use of distributed system clocks, enabling pulses and safety features internal to the system architecture to prevent accidental erasure (REC ENABLE).

The Master Card provides the Bias and Erase pulses required to start the Bias and/or Erase ramp on, and to initiate the completion of the Bias and Erase pulses (ramp off). The Bias and Erase pulses enter through IC42. The record enable command on IC42 allows the proper set enable of IC38 and 39. The Bias and Erase clocks are input to IC41D and IC41A respectively. The output of these devices are connected to IC39 which determines the set or reset of this pulse. These clocks provide a means to determine the rate of the envelope ramp and determine the direction of the ramp to travel (initiation or completion of record). IC36 and 37 provide the up/down count required for initiation of Record as well as completion. The output of the 2 counters provide a 4 bit output that is converted by an R2R ladder network. This provides an envelope amplitude directly proportional to the 4 bit output of IC36 and IC37. This is filtered through IC27 and is the control input to IC26.

IC26 is a constant current 2 quadrant multiplier. The output of IC26 provides an amplitude modulated (AM) signal of 100kHz Erase and 400 kHz Bias drive. These outputs are then routed to IC24 and IC25 (Bias/Record and Erase respectively). The outputs of these amplifiers are sent to Q2 and Q3 (Q4 and Q5). This transistor amplifier increases the erase current to an adequate level. Bias level is controlled by the use of IC21. The command for this level change is performed by the operator via the ALN Panel.

IC23, an analog switch, is a safety device assuring that neither bias or erase can be applied to the respective LEDs without the enable of the record ready signal. In addition, relay K2 provides a redundant safety feature when the record hold signal for the master card is not present. Q6 and the RC time constant of R6 and C161 provide a record relay hold slightly beyond the time of envelope collapse of the bias and erase signals. K2 will energize just prior to the initiation of the erase and bias signals and de-energizes after the envelopes have fully depleted.

Timing of the bias and erase envelope ramps are managed by IC36 and IC37. The timing of IC36 is controlled by the ERASE CLOCK signal from the MST card. IC37 is clocked by the BIAS CLOCK signal from the MST card. IC23 is a digital switch that receives commands from the Q outputs of IC38 and 39 (Ramp Control Circuitry). The external noise reduction control is provided by IC34 and IC44. When the channel card is provided with either a command signal (input or record) the opto isolator IC44 will provide the relay closure required to enable the external noise reduction relay (refer to Section 2 of this manual for interconnection specifications).

The audio input to the CNL card is connected to a thick film differential input stage (IC6). The output of IC6 (input amplifier) is routed (via digital switch IC12). IC12 is not used at this point in time but may be utilized in the future for feature enhancement. The input signal is connected to another digital switch IC14. IC14 determines the input select source. The SLATE BUS is being utilized for the CALibrate IN (CAL IN) signal routing to tracks. The selected signal is then directed to IC7. The output of IC7 provides the input to IC17 (1/2). This provides record level adjustment under user control. The output of IC15 (1/2) output is connected to the other half of IC17 (2/2). This portion of IC17 is used to control the adjustment of record high frequency equalization under user control. The output of IC15 (1/2) is also connected to IC13 (pin 11), a digital switch. IC13 provides the selection of the output of the machine. This selected signal can be INPUT, REPRO or SYNC. The output of IC15 also directs the signal to the Secondary Feed Forward and Feedback Compensation circuit that is controlled by IC16 and 19. The reproduce chain can be

supplied signal from either the REPRO or SYNC head. The input from the heads is selected by K1; K1 receives the command from user selection on the Remote Control Unit. The output of K1 is connected to a ferrite balun for high frequency rejection. The input amplifier of the reproduce chain is an LM394. The LM394 is a instrumentation type amplifier exhibiting very low noise and high gain qualities. The output of Q7 (LM394) is then routed to IC10. The combination of these two devices provide a very efficient common mode rejection input stage. IC1 provides additional gain and buffering to the input of IC5. The combination of IC2 and IC5 manipulate the low frequency equalization and integration required. The second half of IC5 and IC3 provide the high frequency characteristics. Both Low and High frequency equalization are accessible under user control. IC4 is used when various types of head architecture are used. It provides a choice of gap compensations, and control of very low frequency boost control with Low End Modifier (LEM) defeat. This type of control is normally used for 30 IPS response. This control is part of the gap compensation programming. The reproduce or sync signal is then directed from the output of IC3 to IC13 whereby output monitor switching is provided.

The output from IC13 is connected to IC8 which is configured as an inverting buffer. The inverted signal is routed to IC12 (1/2). IC12 is not utilized at this time, but may be implemented in the future. The output of the second half of IC8 is then routed to IC21. This provides the amplitude control of the output monitoring circuit. IC47 and IC32 are used to route the command for dimming of the output circuitry under CPU control. IC46 acts as a driver to IC43 (the opto-isolator). During fast wind modes and Stop, the output of IC8 is turned off by IC43. Dim is approximately 40dB. Dimming can be either individual cards or the entire machine. The output Hybrid (IC11) provides a low output impedance and differential output characteristics. IC9 is used as a meter buffer stage and adjustment of meter calibration.

5.2.5 Audio Motherboard (ADM) Overview/Circuit Description

There is one ADM board mounted at the rear of the audio signal section of the APR-5000. The ADM board contains all of the interconnections of the Channel Cards (CNL), the Time Code Card (TCC), the Master Card (MST) and Audio Logic Control from the CPU. In addition, all audio power and ground lines are routed to the audio signal cards via the ADM. There is no active circuitry on the assembly.

5.2.6 Front End Transformer Board (FEX) Overview

The Front End Transformer Board contains the Record/Sync relay, Bias traps and necessary transformers required to interface the audio electronics of the APR-5000 to the head stack. The FEX board contains three channels of identical electronics. As all channels of electronics on the ADM board are identical, the description of one only channel is necessary.

5.2.7 FEX Board Circuit Description

Transformer T1 is used to provide reduce sync noise when using the record head as a playback head. This is connected via Relay K1. The normally closed contacts of K1 provide the Record Audio and Bias to the Record Head. When energized, K1 then feeds audio from the Record Head to the reproduce circuitry on the Channel Card. (This command is from the CTM.) The Record Drive is connected to an impedance matching network R1, R2 and C1, and then to a bias trap consisting of L1 and C3.

Transformer T2 is used to step-up the bias drive from the CNL Cards to the proper level required. Transformer T3 is once again used to step-up the erase drive to the erase head.

5.2.8 Alignment Board (ALN) Overview

The Alignment Board provides user access to the audio alignment of the APR-5000. Included on the Alignment Board are also the ability for speed change control.

5.2.9 ALN Circuit Description

The basic hardware of the audio control monitor (ACM) and the alignment panel are identical. IC1 is an 8279 programmable keyboard encoder. The encoder program is set upon initial power up via the CPU. The output of the 8279 is connected to two 3 to 8 line decoders. IC4 which acts as a keyboard scan, scans the lines for increment and decrement of alignment features, all record adjustments, reproduce adjustments and equalization. In addition, the return lines are fed back into IC4 and work similar to the ACM board. The second output of IC5 is connected to 8 LEDs.

These Transistors, Q9 to Q14, control the two 7 segment displays that are located within the ALN panel. The output of these 7 segment displays are then connected to 8 additional transistors which are the return lines that are connected directly into the 8279. IC2 and IC3 provide for external control of the alignment signals. In addition, the headstack

pole which is routed from connector CNJ 229 controls the switching of IC2. The headstack pole will indicate either a head off condition, a head air condition or a head invalid condition. A second set of functions which is controlled by a control key input to the 8279 allows the user access of secondary Gap compensations and feed forward and feedback Record compensations.

5.2.10 Audio Control Motherboard (ACM)

The Audio Control Motherboard is mounted horizontally within the meter housing of the APR-5000 Series tape machines. To access this board, open the rear door of the meter housing by removing the upper attaching screws. The door is hinged on the bottom. The ACM is attached to the meter housing assembly by way of Phillips-type screws on the PC board and on the heatsink of the STK457 Hybrid Power Amplifier device. Some early APR-5000 units use Totsu type hardware. This may be removed with a special Totsu-type screwdriver or by carefully using a standard flat blade screwdriver. Newer units utilize Phillips-type hardware.

5.2.10.1 ACM Functions

The ACM (Audio Control Motherboard) contains the circuitry that controls the audio mode switching and power amplifier in the APR-5000 meter housing. This board consists of an 8279 Programmable Keyboard/Display Matrix Encoder interface, a set of 74LS138 decoders, and other control logic. In addition, an STK457 hybrid Stereo Power Amplifier is included. This amplifier is capable of driving two individual speakers through the HEADPHONE jack on the front panel of the machine. In the factory configuration, the stereo amplifier outputs (coming from the HEADPHONE jack) are summed by a resistor network to drive only one speaker mounted in the meter housing. The feeds to this speaker are normalized through the headphone jack on the front panel of the machine. Whenever a stereo headphone plug is inserted, the two individual outputs of the hybrid Power Amplifier are routed to the right and left headphone outputs and the speaker is isolated (disconnected).

5.2.10.2 ACM Circuit Description

The circuit description centers around the 8279 Programmable Keyboard/Display Matrix Encoder (IC5). This sets the audio status buffers in an X-Y pattern or a matrix. Normally, this device detects when either a key is pressed within the meter housing or when a command from the CPU enables a function within the network housing. In the case of a keypress, the 8279 will provide a unique code to the CPU indicating which of the keys was pressed. This is of course accompanied with an interrupt signal (1RQ) to be fed to the CPU.

When the CPU reads the 8279, the READ (RD) and CHIP SELECT (CS) lines go LOW and receives the data from the 8279. Return lines also are fed via 2 sets of CD4016 digital switches IC8 and IC9. The command for these digital switches can be external as on a channel status or a remote controller unit.

When writing to the 8279, the WRITE line (WR) goes LOW and the S0 through S2 outputs of the 8279 are fed to two 74LS138 (3-to-8 line decoders). ICs 3/4 in addition, an address line is selected causing the chip select line (CS) on the 8279 to go to a LOW true state. The outputs of the 74LS138 drive two sets of lines. This first set is key seeking the second LED illustrations of those keys.

IC3 drives the keyboard scan line for all of the keys located on the meter housing. The return line for the keyboard is then fed back to the 8279.

IC4 drives the LED row lines. This is fed via a 74HC04 IC6 to provide proper logic level drive and isolate the LED drive from the output of the 8279. The LED column lines are then fed to the 8279. The mute switching lines for the monitor speaker are fed from the Mute Switching Board (MSB) to a flip-flop located on the ACM. IC2 (MC14013 or 4013) latches the information for the MSB. The output of the 4013 is then fed to a DG212 Digital Switch (IC1). These are the command lines to turn the LEDs located within the mute keys on and off. In addition, IC1 also routes a feed from the meter drive output to the audio attenuator located in the meter housing. The commands for both the Mute Switching Board (MSB) audio attenuator are in parallel.

5.2.10.3 Power Amplifier

The power amp located within the circuitry of the ACM can provide the drive for two independent speakers. The inputs to IC10 are from the audio attenuator previously described. In the standard APR-5002 or APR-5003/APR-5003V, one speaker is included. Notice that there is a passive resistive summing network which is connected by way of jumpers. The jumpering arrangement may be changed such that the summing resistors are disconnected providing two separate speaker feeds. Also notice that the connector for the second speaker is provided on the ACM.

The STK457 is the Hybrid Stereo Power Amplifier. The input is fed via pin 16 for the left channel (CH-1) or pin 1 for the right channel (CH-2). In the right channel circuit, resistor R18 and capacitor C15 provide insulation of the attenuator and AC coupling to the input of the amplifier. Capacitor C13 provides high frequency decoupling to the input. The network of R16 and R12 determines the gain of the amplifier. R11 is used to provide a continuous load source for the outputs. The networks of C12, R13 and C14, R7, determine the low and high frequency roll-off points of the amplifier. The output of the amplifiers are fed first to the headphone jack located on the front panel of the APR-5000. This is a normalizing jack which feeds the signal to the speakers via a load resistor if no headphone plug is installed. When a plug is inserted into the headphone jack, the amplifier outputs feed to the headphones and the meter housing speaker(s) become disconnected.

5.2.11 Control Meter Board (CTM)

The Control Meter (CTM) assembly contains all of the switches and controls relating to one audio channel in the meter bridge. In addition, the VU meter is located on the assembly. The CTM is, of course, located in the meter housing. Since there is one CTM for each audio channel, one is installed in the APR-5001 meter housing or two on the other APR-5000 Series machines.

5.2.11.1 CTM Circuit Description

The VU meter receives its drive from the audio Channel (CNL) card via the cardcage motherboard (ADM) through a wiring harness to the Audio Control Motherboard (ACM) mounted in the bottom of the meter housing. The adjustment for the calibration of the VU meter is made by adjusting the gain of the meter buffer amplifier located on the Channel Card (CNL).

Transistors Q1 and Q2 provide the drive current to turn on the BIAS and ERASE indicator LEDs when a LOW true level signal is present at the base.

The diode and switch matrix of diode D1 through D6 and switch S1 through S6 form the keyboard matrix array controlled by an 8279 Programmable Keyboard/Display Matrix Encoder. The switches are the momentary contact type. These connect the strobe pulse output of the 8279 to the 8279 keyswitch input. The 8279 is located on the Audio Control motherboard (ACM).

IC1 and IC2 are configured to provide the LED row/column configuration needed by the 8279 IC. Diodes D7 - D13 limit the current flow in one direction from the 74HC08 (IC1). When both inputs of the 74HC08 are high, this produces a high on the output thus causing conduction of the FET Driver.

FET transistors Q3 through Q9 provide the drive current required to turn on the LED. R12 through R18 are current limiting resistors for the LEDs located within the switch assembly. The resistor and capacitor on each gate of the FET provides the proper bias for turn on.

5.2.12 Time Code Channel Card (TCC)

The Time Code Channel Card (TCC) is located in the card rack which can be accessed by lowering the ALN panel. Cards may be removed (with power OFF) using the card edge attachment. Each of the slots in the card cage are designated for specific purposes. The lowest slot is always used with the Master Card (MST). The next slot above the MST is used for audio Channel 1 (Left), then audio Channel 2 (Right), and Time Code Channel 3 (Center track - Time Code).

5.2.12.1 Principles of Operation

The Time Code Channel Card (TCC) combines all of the Record/reproduce circuitry and performs all audio processing for the Time Code Channel of the APR-5003 and APR-5003V machines. The TCC will not be found in APR-5001, APR-5002 or APR-24 machines.

5.2.12.2 TCC Control Circuit Description

Note that this circuit is identical to that of the Channel Cards for the audio channels with the exception of some minor changes in some of the resistor and capacitor component values. The component changes have been performed so that the TCC is optimized for the handling of the time code data signal. Since this card is designed for use with time code, it is specifically optimized for the recording and reproducing of serial digital data at the time code data frequency range. Also note that the output of the TCC is fed to the CPU time code reader (PB TC). No time code generator or reader functions are performed on the TCC.

The control of the TCC originates from the CPU. The data generated by the CPU flows to the Local/Network Transceiver board (LNT) to the audio sub-system which includes a number of Channel Cards, a Time Code Channel Cards and a Master Card (MST). Direct control of the TCC is performed by the Master Card (MST). The Master Card (MST) converts the commands from the CPU to the audio control address/data bus. This bus is made up of 8-bits of data and an Address data that controls a precoded (hardware addressed) set of parameter enables and channel enables. (In the case of a multi-track tape machine like the APR-24, drawer enables signals are also present. However, in this case, these are used only by CNL cards since there are no TCC cards utilized in the APR-24.)

The pre-encoded parameter enables allow latching of selected data to the appropriate latches on the TCC card. Some data is fed to the multiplying D/A Converters which are adjustment devices in the alignment circuitry. Data buffer (IC28) latches the data (from the MST) that represents the resistance provided by a multiplying D/A. Each D/A is installed in the gain structure of the equalizer/filter or amplifier circuits on the TCC card. On the Master Card, the data is latched when the WRBS pulse goes LOW.

Additionally, the PA or Parameter Enables (IC32) subsequently are decoded into the parameters such as INPUT calibration, BIAS calibration, REPRO EQ, REPRO LVL, SYNC EQ, SYNC LVL, Secondary Compensation, and Gap Compensation. These independently become enabled when the chosen parameter line goes LOW (IC33).

IC29 latches the data for Secondary Gap Compensation control, UNCAL (INPUT and OUTPUT), RECORD Enable, DIM INHIBIT and other frequency related switching functions (LEM Defeat, etc.). Note that many of these functions are disabled by way of the software. The hardware which supports these functions is still installed on the TCC due to other functions which are used.

IC30 latches mode functions that allow the control of Repro/Sync routing to the reproduce chain DIM circuit, calibration input switching, individual REPRO/SYNC switching. Most of the functions controlled by this device on the CNL are not supported by the software due to the fact that this card supports the center track time code channel which does not need to utilize the various functions.

IC31 provides the latching of data for Secondary RECORD Compensations as well as Bias and Record Ramp timing. This is accomplished by the use of distributed system clocks, enabling pulses, and safety features internal to the system architecture to prevent accidental erasure (bias inhibit).

5.2.12.3 TCC Bias and Erase Circuitry

The Master Card provides the Bias and Erase pulses required to start the Bias or Erase ramp and to initiate the completion of the Bias and Erase pulses. The Bias and Erase pulses enter through IC42. The RECORD enable command on IC42 allows the proper set enable of IC38 and IC39. The inputs to IC41 are the Bias and Erase clocks. The output of these devices are fed to IC39 which determines the set or reset of this pulse. These clocks provide a means to determine the rate of the envelope ramp and determine the direction of the ramp to travel (initiation or completion of RECORD).

IC36 and IC37 provide the up/down count required for initiation of RECORD as well as completion. The output of the 2 counters provide a 4-bit output that is converted by an R2R ladder network. This provides an envelope amplitude directly proportional to the 4-bit output of IC36 and IC37. This is filtered through IC27 and is the control input to IC26. IC26 is a constant current 2 quadrant multiplier.

The output of IC26 provides an amplitude modulated signal (AM) of 100kHz Erase and 400kHz Bias drive. These outputs are then fed to IC24 and IC25 (Bias/RECORD and erase respectively). The outputs of these amplifiers are fed to transistors Q2 and Q3 (Q4 and Q5). This transistor amplifier increases the erase current to an adequate level. Bias level is controlled by the use of IC21. The command for this level change is done via the ALN panel under user program control. These changes are stored in RAM memory on the CPU card and transferred to the TCC via the LNT board and MST card.

IC23, an analog switch, is a safety device assuring that neither bias or erase can be applied (illuminating the respective LEDs) without the enable of the RECORD READY signal. In addition, relay K2 provides a redundant safety feature turning off the recording process when the RECORD HOLD signal for the Master Card is not present.

Q6 and the RC time constant of R6 and C161 provide a RECORD HOLD signal for the relay slightly beyond the time of extinguishing of the bias and erase ramps. K2 will energize just prior to the initiation of the erase and bias ramps and de-energizes after the ramps have depleted.

Timing of the bias and erase ramps are handled by IC36 and IC37. This receives a clock from the Master Card. IC23 is a digital switch that receives its commands from the Q outputs of IC38 and IC39 (Ramp Control Circuitry).

5.2.12.4 TCC Noise Reduction Circuitry

The external noise reduction control is provided by IC34 and IC44. Since this card is used for the Time Code Channel, the function of the noise reduction circuitry is disabled and no external connection for channel 3 is available.

5.2.12.5 TCC Audio Circuitry

The audio input to the Time Code Channel Card is fed to a thick film differential input. The output of IC6 (input amplifier) is routed via digital switch IC12 (1/2). This provides an input (UNCAL) control by selecting either the internal calibration (signal fed to the UNCAL potentiometer) or the external signal coming back from the UNCAL vernier control on the TCM (in the meter housing) via IC7. The input signal is fed to another digital switch IC14. IC14 determines the input select source. The SLATE output is the input to the input calibration port on the rear panel of the machine via the MST card amplifier circuitry. The signal is then fed to IC7. The output of IC7 provides the input to IC17 (1/2). This provides RECORD level adjustment under user control from the ALN. IC15 output is then fed to the other half of IC17 (2/2). This portion of IC17 is used to control the adjustment of RECORD high frequency equalization under user control from the ALN.

The output of IC15 is then fed to IC13, a digital switch. IC13 provides the selection of the output of the machine. These selections can be input, reproduce or sync. The output of IC5 also routes to the Secondary Feed Forward and Feedback Compensation that is controlled by IC16 and IC19 and is preset by the software (not adjustable for the time code track). The output of IC18 is again fed to IC13.

The reproduce chain is always fed from the time code head. The input is coupled through a ferrite balun for high frequency rejection. The input amplifier of the reproduce chain is a LM394. The LM394 is an instrumentation type amplifier exhibiting very low noise and high gain qualities. The output of Q7 (LM394) is then fed to IC10. The combination

of these two devices provide a very high common mode rejection input stage. IC1 provides additional gain and buffering to the input of IC5. The combination of IC2 and IC5 provide the low frequency equalization and integration required.

The second half of IC5 and IC3 provide the high frequency characteristics. IC4 is used when various types of head architecture are used. It provides several different gap compensations by switching capacitors in the circuit. Provided also is control of very low frequency boost control with Low End Modifier (LEM) defeat. These circuits are not supported by the software since the time code channel does not require these functions (the TCC is dedicated to the center track time code channel which basically only uses one type of head and a fixed gap compensation).

The time code signal is then fed from the output of IC3 to IC13 which usually performs the output monitor switching function. This function is also not supported by the software due to the fact that there is only one time code head.

The output from IC13 is then fed to IC8 and then to IC12 (1/2). IC12 provides a time code output to be fed to the CPU (in the transport assembly). The output of the second half of IC8 is then fed to IC21. This provides the amplitude control of the output monitoring circuit. IC47 and IC32 are used to route the command for dimming of the output circuitry under CPU control (another function not used for the TCC). IC46 acts as a driver to IC43 opto-isolator.

The Differential Line Output Hybrid (IC11) provides a low output impedance and differential output characteristics. IC9 is used as a meter buffer stage and adjustment of meter calibration.

5.2.13 Time Code Meter Board (TCM)

The Time Code Meter Board contains all of the switches and controls relating to the status of the Center Track Time Code Channel. The assembly will only be found on the APR-5003 Series machines, located in the meter housing. In addition, the VU meter is located on the assembly.

5.2.13.1 TCM Circuit Description

The VU meter receives its drive from the TCC card via the cardcage motherboard (ADM) through a wiring harness to the Audio Control Motherboard (ACM) found in the meter housing. The adjustment for the calibration of this meter is made by adjusting the gain of the meter buffer amplifier located on the Time Code Channel Card (TCC).

Transistors Q1 and Q2 provide the drive current to turn on the RECORD and erase LEDs when a LOW true level signal is present at the base.

The diode and switch matrix of diodes D1 through D6 and switches S1 through S6 form the keyboard matrix for the 8279 Programmable Keyboard/Display Matrix Encoder on the ACM. The switches are the momentary contact type with normally open contacts. These connect one of the strobe lines to one of the keyswitch return lines of a circuit controlled by an 8279 Programmable Keyboard/Display Matrix Encoder which is located on the ACM.

IC1 and IC2 are configured to provide the LED row/column configuration needed by the 8279 IC. Diodes D7 - D13 limit the current flow in one direction from the 74HC08 (IC1). When both inputs of the 74HC08 are high, this produces a high on the output thus causing conduction of the FET Driver.

FET transistors Q3 through Q9 provide the drive current required to turn on the LED. Resistors R12 through R18 are current limiters for the LEDs located within the switch assembly. The resistor and capacitor on each gate of the fet provides the proper bias for turn on.

5.2.14 APR Head ID Board (AHB) Description

The APR Head Identification board (AHB) is mounted in the headstack assembly of both the APR-5000 Series tape machines. (The APR-24 utilizes this board but it is mounted remotely from the headstack assembly.) It contains the 8-bit DIP switch which is used to provide a unique identity code to the headstack. Using this code, the machine calls up the appropriate set of preset alignments from memory.

This DIP switch is only read upon initialization of the CPU (such as power-up of the machine or reset of the CPU board).

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**SECTION 6
MAINTENANCE
AND
CALIBRATION PROCEDURES**

6.0 Overview

This section provides the information required to perform routine maintenance, full transport and audio electrical alignment, and mechanical adjustment of the APR-5000. These procedures are formatted to facilitate a systematic approach to a complete alignment of the APR-5000. In some cases of major parts replacement it may be necessary to deviate from the order of the procedures as given. If a major part or assembly is to be replaced, refer to Section 6.3 ADJUSTMENTS AFTER MAJOR PARTS REPLACEMENT and Appendix G MAJOR PARTS REPLACEMENT.

The APR-5000 is designed to give dependable service throughout the life of the machine. However, as with all electro-mechanical devices the APR-5000 requires routine maintenance to perform at full potential. Section 6.2 ROUTINE MAINTENANCE lists all necessary adjustments and their approximate intervals.

6.1 Necessary Tools

The following is a complete list of test equipment and tools required to perform maintenance or repair of the APR-5000. The test equipment marked with an asterisk (*), standard technician tools, cleaning supplies (Section 6.1.3), and the appropriate test/alignment tapes (Section 6.1.4) are the basic tools necessary for regular preventative maintenance and alignment. If it is desired to substitute the test equipment listed, the substitute test equipment should have equivalent or better specifications than the equipment listed below.

6.1.1 Test Equipment

Demagnetizer*.....	NORTRONICS Model No. QM-211
Oscilloscope.....	Tektronix 455, 60MHz, Dual Trace, Delayed Sweep
AC Voltmeter*.....	Senheiser UPM-550
Signal Generator*.....	Krohn-Hite 1000A, or Hewlett Packard 209
Frequency Counter*.....	Hewlett-Packard 5381A
Digital Voltmeter.....	Fluke 77, or Beckman 310
Logic Probe.....	(optional)
Flutter Meter.....	EMT 424 (optional)
Wave Analyzer.....	Hewlett-Packard 3581A

6.1.2 Service Tools

Technician Tools.....	U.S. inch and metric standard
Spring Scale 200g.....	Sony #J-6041-630-A
5kg.....	Sony #J-6041-640-A
Metric Nutdriver Set.....	4mm to 13mm
Metric Hexdriver Set.....	Including the following sizes: 1.5mm, 2mm, 2.5mm, 3mm Sony #7-700-736-00
U.S. Standard Hexdriver Set.....	Including the following sizes: 1/8-inch, 7/64-inch Sony #J-7100-040-A
Tentelometer (T2-H12-2).....	Sony #J-6041-680-A
Zenith Block.....	Sony #J-6105-960-A
Rack Gauge.....	Sony #J-6105-980-A
Roller Guide Alignment Tool.....	Sony #J-6105-930-A
Brake Torque Hub Fixture.....	Sony #J-6101-430-A
Reel Height Gauge.....	Sony #J-6105-930-A
Torque Driver.....	Sony #J-6103-860-A
Time Code Decoder Fixture.....	Sony #J-6106-140-A
Center Track Time Code Head Gauge.....	Sony #J-6220-320-A
Spring Scale (5kg).....	Sony #J-6041-640-A
Spring Scale (1kg).....	Sony #J-6042-670-A

For additional test equipment and tool information contact your local dealer or service representative for assistance. Below is a space provided for listing the phone number of the Sony Regional Service Representative nearest you.

REGIONAL SONY
SERVICE
REPRESENTATIVE: _____

6.1.3 Cleaning Items

Lint-Free Cleaning Cloth.....(Chamois cloth, etc. for general cleaning of the machine)

All-purpose Non-detergent Household Cleaner.....For use in general cleaning of the machine.

Cleaning Piece.....(Sony #2-034-697-00, Foam swabs, or photographic grade chamois for cleaning of the polished surfaces of the machine)

Cleaning Fluid.....(Sony #Y-2031-001-0, Methanol, or Commercial Grade Alcohol for use with the Cleaning Piece on the fine polished surfaces of the machine)

Before beginning the cleaning of the APR-5000, refer to the cleaning procedures and precautions given in Section 6.4
CLEANING AND DEMAGNETIZING.

6.1.4 Test Tapes

To properly align the APR-5000 playback electronics, precision test tapes must be used. These tapes, manufactured under controlled laboratory conditions, contain a series of test tones at a standard reference fluxivity. The tapes that are suggested for use are standard reference tapes manufactured by Magnetic Reference Laboratory (MRL). In order to retain the integrity of these tapes, it is important to handle the tape with care. Never store the tapes near any magnetic fields, transmitters, or expose them to extreme temperature or humidity. Store them as you would a master tape.

Whenever it is necessary to use any of these tapes, always clean and demagnetize the headstack prior to using the reference tapes. For best results with the test tapes, ensure that the tape is packed evenly on the reel before beginning the alignment procedure. Since the test tapes are stored in the "TAILS OUT" position, REWIND mode can be used to ensure a "good pack".

NOTE: The high frequency tones recorded on the test tapes will drop several decibels as the tape ages. Test tapes should be closely monitored and replaced if undesirable deterioration exists.

Magnetic Reference Laboratory (MRL)

Reference Fluxivity (250nWb/meter)

1/4-inch Tapes

MRL #21T204 7.5ips NAB
MRL #21T302 7.5ips IEC
MRL #21J205 15ips NAB
MRL #21J303 15ips IEC
MRL #21L221 30ips AES
MRL #21F101 3.75ips
NAB/IEC

1/2-inch Tapes

MRL #31T218 7.5ips NAB
MRL #31T328 7.5ips IEC
MRL #31J219 15ips NAB
MRL #31J339 15ips IEC
MRL #31L220 30ips AES

Table 6-1. Recommended Test Tapes

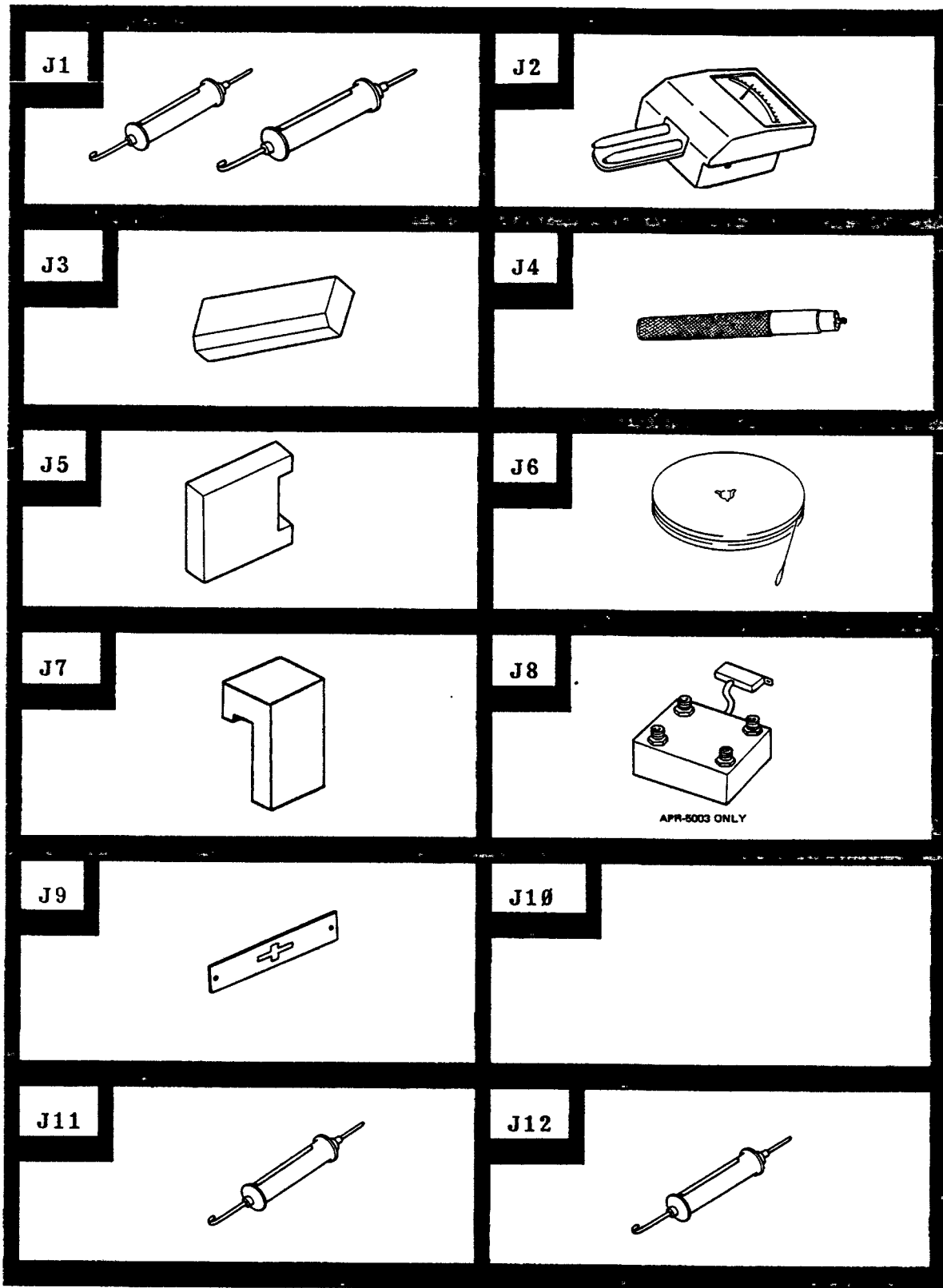


Figure 6-1. Jigs and Fixtures

ILLUSTRATION #	DESCRIPTION	PART NUMBER
J1	SPRING SCALE 1kg	J-6042-670-A
	SPRING SCALE 5kg	J-6041-640-A
J2	TENVELOMETER (T2-H12-2)	J-6041-680-A
J3	ZENITH BLOCK	J-6105-960-A
J4	ROLLER HEIGHT FIXTURE	J-6105-930-A
J5	RACK GAUGE	J-6105-980-A
J6	BRAKE TORQUE HUB FIXTURE	J-6101-430-A
J7	REEL HEIGHT GAUGE	J-6105-930-A
J8	TIME CODE DECODER FIXTURE	J-6220-320-A
J9	CENTER TRACK TIME CODE GAUGE	J-6220-320-A
J10	TORQUE DRIVER	J-6103-860-A
J11	500g SPRING SCALE	7-732-050-50
J12	200G SPRING SCALE	7-732-050-40

Table 6-2. Test Jig Description and Part Numbers

6.2 Routine Maintenance

The APR-5000 is designed to minimize maintenance. The most important preventative maintenance is regular cleaning and demagnetizing, as described in Section 6.4 CLEANING AND DEMAGNETIZING. Perform the following maintenance at the specified intervals.

PREVENTATIVE MAINTENANCE	PROCEDURE SECTION	TIME INTERVAL BETWEEN MAINTENANCE*
Clean Tape Path	6.5	10 Hours
Demagnetize Heads	6.5	20 Hours
Clean Moving Guides	6.5	100 Hours
Tape Tension	6.6.6.2	500 Hours
Check Reel Motor Brakes	6.5.1	1000 Hours
Check Head Wear	Appendix F	1000 Hours
Renew Hours Meter	Oper./Maint.Manual Sect.4.4 pg.4-3	5000 Hours
* = Equivalent Playing Time at 15ips		

Table 6-3. Preventative Maintenance Schedule

6.3 Adjustment After Major Parts Replacement

After a major part or assembly has been replaced it is important that the APR-5000 alignments relating to that specific area be checked and, if necessary, adjusted to accommodate for the new part or assembly. Refer to the following check/adjustment procedures when installing new major parts or assemblies.

6.3.1 Adjustments After Head Replacement

- 1) Mechanical Height and Zenith Adjustment: Appendix F
- 2) Electro-mechanical Head Alignment: Section 6.6.1
- 3) Repro/Sync Calibration Check/Adjustment: Section 6.6.4 and Section 6.6.5

6.3.2 Adjustments After Reel Motor Replacement

- 1) Turntable Height Check/Adjustment: Appendix F
- 2) Emergency Braking Adjustment: Appendix F
- 3) Reel Tach Sensor Adjustment: Section 6.5.5
- 4) RMD Board Adjustment: Section 6.5.6

6.3.3 Adjustments After Capstan Motor Replacement

- 1) Play Tape Path Check/Adjustment: Appendix F
- 2) Flutter Check/Adjustment: Section 6.6.7

6.3.4 Adjustments After Roller Guide Replacement

- 1) Wind Speed Tape Path Check/Adjustment: Appendix F
- 2) Play Speed Tape Path Check/Adjustment: Appendix F
- 3) Flutter Check: Section 6.5.7.1
- 4) Mechanical Head Alignment Check/Adjustment: Appendix F

6.3.5 Adjustments After CNL Card Replacement

- 1) CNL Card Internal Alignment Check/Adjustment: Section 6.8.1
- 2) Meter Calibration Check/Adjustment: Section 6.6.3
- 3) Repro/Sync Level Calibration Check/Adjustment: Section 6.6.4
- 4) Repro/Sync High Frequency Calibration Check/Adjustment: Section 6.6.5

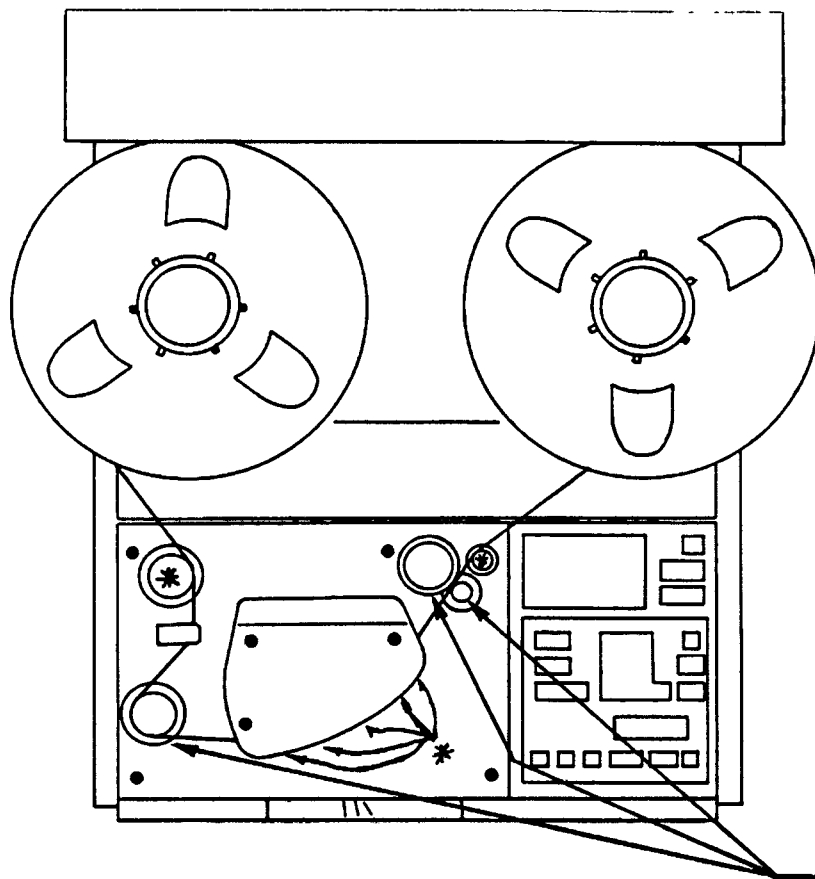
6.4 Cleaning and Demagnetizing

6.4.1 General Notes on Cleaning

Before attempting the alignment procedures all tape guides and heads should be thoroughly cleaned and demagnetized. Cleaning fluid or methanol (commercial cleaning alcohol) is applied with foam swabs or photographic grade chamois to clean the specified parts, refer to Figure 6-2 for parts location. When cleaning the capstan or the moving guides refer to the specific sections for these procedures (Section 6.4.2 and 6.4.3).

****NOTE: DO NOT USE CLEANING FLUID (METHANOL) ON THE PINCH ROLLER, CAPSTAN SHAFT, OR THE TIMER ROLLER. CLEANING THE PINCH ROLLER OR TIMER ROLLER WITH THE CLEANING FLUID WILL DETERIORATE THE RUBBER. CLEANING THE CAPSTAN SHAFT WITH THE CLEANING FLUID IS USELESS AS THE CLEANING FLUID WILL NOT REMOVE THE DEEP DISCOLORATION THAT OCCURS WITH HEAVY MACHINE USE.**

* Use Methanol
(or equivalent)



Use Non-detergent
Cleaner Here

Figure 6-2 Parts to be Cleaned

6.4.2 Capstan Cleaning

Necessary Tools: -Lint-free Cleaning Cloth (or cotton swabs)
-All-purpose Non-Detergent Household Cleaner

When cleaning the capstan it is extremely important that the cleaning solution (non-detergent household cleaner) does not drip into the upper bearing. In order to avoid damage to the bearings during cleaning, follow the procedure shown below.

- STEP 1** Turn the power switch ON.
- STEP 2** Remove the tape (if any) from the machine.
- STEP 3** Remove the pinch roller.
- STEP 4** Place an opaque object across the EOT sensor.
- STEP 5** Engage DUMP EDIT Mode.

STEP 6 As shown in Figure 6-3, place two swabs (the upper swab moistened with the cleaning solution and the lower swab dry) onto the spinning capstan shaft.

STEP 7 While applying light pressure to the swabs, move the swabs in a vertical motion (as shown in Figure 6-4).

****NOTE: BE SURE THAT NONE OF THE CLEANING SOLUTION ENTERS INTO THE BEARINGS. IF THE CLEANING SOLUTION DOES ENTER INTO THE BEARINGS THE LIFESPAN OF THE MOTOR WILL BE DRASTICALLY REDUCED.**

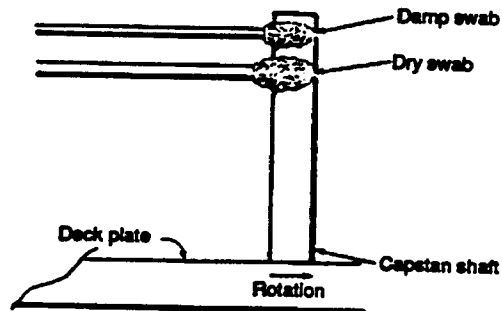


Figure 6-3. Recommended Cleaning Swab Placement

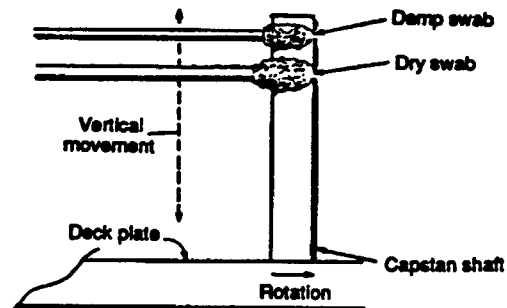


Figure 6-4 Capstan Shaft Cleaning

6.4.3 Demagnetizing the Tape Path

Necessary Tools: Demagnetizer

The heads and the tape guides should be routinely demagnetized since, after only a few hours it is possible for these surfaces to become slightly magnetized. In extreme cases, a tape passing over a magnetized head or tape guide will be partially erased. The following procedure should be applied at the specified service interval (refer to Table 6-2).

- STEP 1 Turn the APR-5000 power switch OFF.
- STEP 2 Turn the demagnetizer power switch ON.
- STEP 3 Beginning with the Erase head, start a circular motion with the demagnetizer approximately 18-inches (46-cm) away from the front of the head. Continuing the circular motion, move the demagnetizer to within 1/16-inch without touching the head.
- STEP 4 While continuing the rotation of the demagnetizer slowly move the demagnetizer away from the head until the distance between the head and the demagnetizer equals approximately 3-feet.
- STEP 5 Turn the demagnetizer power OFF.
- STEP 6 Repeat STEPS 1 through 5 for the Sync head and the Repro head.

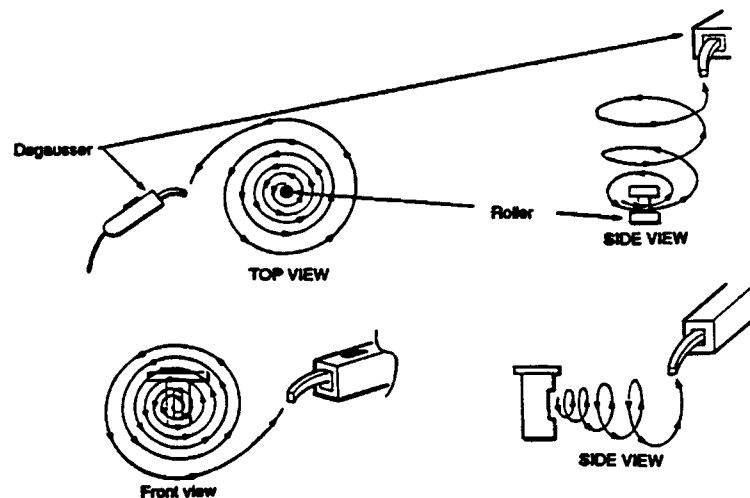


Figure 6-5. Demagnetizing Technique

6.4.4 Cleaning the Moving Guides

Necessary Tools: Cleaning Piece.....(Sony #2-034-697-00)
Cleaning Fluid.....(Sony #Y-2031-001-0)

As with the fixed guides, heads and capstan, the roller guides should be cleaned and demagnetized periodically (refer to Table 6-2). Remember that the roller guides incorporate lubricated bearings in their assemblies. It is very important that the cleaning solution does not enter the bearings as the lubrication will be washed out and the roller guide will have to be replaced.

STEP 1 Turn the **APR-5000** power switch OFF.

STEP 2 Remove all of the roller guides, and place aside in the order in which they were removed from the transport (this will allow exact replacement of the roller guides to their original positions on the transport).

NOTE: If desired, the roller guides can be removed and cleaned one at a time.

STEP 3 Clean all components of the roller guide assemblies carefully ensuring that the cleaning fluid does not enter into the bearing assemblies.

STEP 4 Replace all roller guides onto the transport.

6.5 Transport Check and Alignment Procedures

This section provides the information required to perform a routine transport alignment of the APR-5000. The procedures include check and alignment of the transport mechanical assemblies, and the transport servo system. For tape path alignment procedures and troubleshooting information, refer to Appendix F of this manual.

6.5.1 Reel Motor Assembly Check/Adjustment Procedure

Necessary Tools:

- Phillips Head Screwdriver
- Torque Driver (Sony # J-6103-860-A)
- 500g Spring Scale (Sony # 7-732-050-50)
- 200g Spring Scale (Sony # 7-732-050-40)

Prerequisite: NONE

Specification:

- Supply side brake tension:

Counterclockwise Rotation = 360g (+/-80g)
Clockwise Rotation = 80g (+/-40g)

- Take-up side brake tension:

Counterclockwise Rotation = 80g (+/-40g)
Clockwise Rotation = 360g (+/-80g)

NOTE: When using a 50mm brake torque fixture (#9-911-041-01) the specifications for adjustment are doubled.

360g (+/-80g)—————>720g (+/-160g)

80g (+/-40g)—————>160g (+/-80g)

These procedures need only be performed if there is a part or assembly changed in the brake tension arm assembly (i.e. a new spring installed, new reel motor assembly installed, etc.).

STEP 1 Remove the tape and reels (if any) from the APR-5000 and turn the power switch OFF.

STEP 2 Place the brake torque fixture (#J-6101-430-A) onto the supply reel motor turntable.

STEP 3 Attach the 500g spring scale (#7-732-050-50) to the brake torque fixture string.

- STEP 4** Pull the spring scale so that the reel motor rotates in the counterclockwise direction. Observe the scale reading at the point at which the reel motor begins to rotate. Perform this action several times to attain an average reading. The average reading should be 360g (+/-80g).
- STEP 5** If the reel motor brake torque is not within specification, remove the top rear cosmetic cover (the cover for the TIB board) and adjust the brake spring tension as shown in Figure 6-6.
- STEP 6** Remove the 500g spring scale from the brake torque fixture and replace it with the 200g spring scale (#7-732-050-40).
- STEP 7** While observing the reading on the spring scale, pull the scale such that the reel motor rotates in the clockwise direction. Observe the scale reading at the point at which the reel motor begins to rotate. Perform this action several times to attain an average reading. The average reading should be 80g (+/-40g).

NOTE: Since both the clockwise and counter-clockwise torque of the reel motor brake assembly are adjusted by the same spring, both readings will be interactive. Hence, if the clockwise direction is adjusted the counter-clockwise direction is also adjusted.

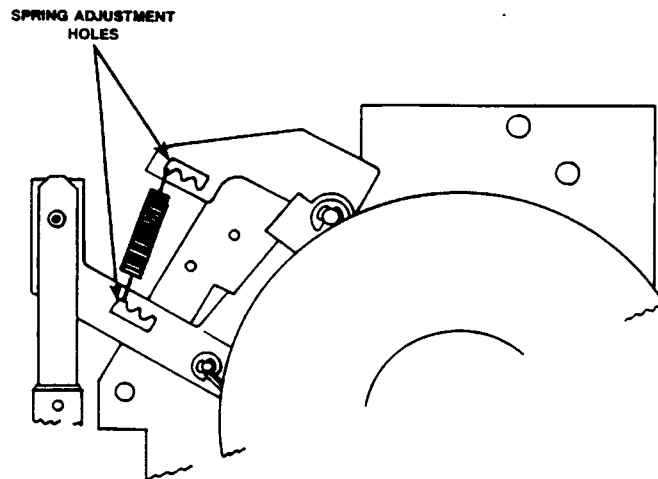


Figure 6-6. Reel Motor Brake Assembly Spring Adjustment

- STEP 8** Remove the brake torque fixture from the supply reel motor and install onto the take-up reel motor turntable.
- STEP 9** Attach the 500g spring scale (#7-732-050-50) to the brake torque fixture string.
- STEP 10** Pull the spring scale so that the reel motor rotates in the clockwise direction. Observe the scale reading at the point at which the reel motor begins to rotate. Perform this action several times to attain an average reading. The average reading should be 360g (+/-80g).
- STEP 11** If the reel motor brake torque is not within specification, remove the top rear cosmetic cover (the cover for the TIB board) and adjust the brake spring tension as shown in Figure 6-6.
- STEP 12** Remove the 500g spring scale from the brake torque fixture and replace it with the 200g spring scale (#7-732-050-40).
- STEP 13** While observing the reading on the spring scale, pull the scale such that the reel motor rotates in the counter-clockwise direction. Observe the scale reading at the point at which the reel motor begins to rotate. Perform this action several times to attain an average reading. The average reading should be 80g (+/-40g).

6.5.2 Reel Turntable Height Check/Adjustment Procedure

Necessary Tools:

- 2mm Hex Driver
- Phillips Head Screwdriver
- Torque Driver (Sony # J-6103-860-A)
- Reel Motor Height Gauge (Sony # J-6105-930-A)

Prerequisite: NONE

Specification:

There shall not be a gap exceeding 0.0005-inch between either the gauge and the reel turntable or the gauge and the reel motor mounting plate. Refer to Figure 6-7.

- STEP 1** Remove any tape and/or reels from the APR-5000 and turn the power switch OFF.

- STEP 2** Remove the upper rear cosmetic panel. This will expose the reel motor mounting plate.
- STEP 3** Place the reel motor height gauge on the reel motor mounting plate as shown in Figure 6-7. Ensure that the reel motor turntable height meets the specification criteria.
- STEP 4** If adjustment is necessary, loosen the set screws (2) with the 2mm hex driver. Adjust the turntable height as required.

6.5.3 Hours Meter Renewal Procedure

Necessary Tools:

- Phillips Head Screwdriver
- Torque Driver (Sony # J-6103-860-A)

Prerequisite: NONE

Specification:

When the Hours Meter reaches the end of its cycle (5000H) it should be replaced. However, if the user prefers, the meter can be operated in the reverse direction by reversing the two leads to the meter. If reverse direction performance of the hours meter is desired, perform the procedure shown in the steps to follow.

- STEP 1** Turn the APR-5000 power switch OFF.
- STEP 2** Open the ALN panel door. Remove the two securing screws from the front of the power supply door and open. The power supply door is hinged on the bottom edge.
- STEP 3** Remove the timer connector at CNJ-464 of the CSL board. Rotate the connector 180-degrees and install back onto the male connectors. This reversal of the signal feed to the timer will cause the meter to "count backward" from 5000H to zero hours.
- STEP 4** Close the power supply door and install the securing screws. Turn the power switch ON.

6.5.4 Shield Assembly Check/Adjustment Procedure

Necessary Tools:

- Philips Head Screwdriver
- Work Tape
- Flat Blade Screwdriver

Prerequisite: NONE

Specification: Shield assembly should operate smoothly.

The shield assembly on the APR-5000 is designed for minimal maintenance and adjustment requirements. There is only one point to check on this assembly. The point of check (and if needed, adjustment) is the dashpot dampening adjustment. These procedures need only be done if the dashpot or shield spring are replaced.

6.5.4.1 Shield Assembly Check Procedure

- STEP 1 Turn the APR-5000 power switch ON.
- STEP 2 Load and thread the work tape onto the machine.
- STEP 3 Press the PLAY key. This will put the APR-5000 into PLAY mode.
- STEP 4 While the machine is in PLAY mode, press the SHIELD DEFEAT key. This will lower the shields.
- STEP 5 While continuing in PLAY mode, press the SHIELD DEFEAT key. This will raise the shields.
- STEP 6 Repeat STEPS 4 and 5 several times to ascertain an average operation performance of the shield assembly.
- STEP 7 If the shield assembly is not performing within specification, perform the adjustment procedure listed in Section 6.6.4.2.

6.5.4.2 Shield Assembly Adjustment Procedure

- STEP 1 Turn the APR-5000 power switch OFF.
- STEP 2 Remove the top panel as shown in Section 6.4.2 (page 6-3) of the Operation and Maintenance Manual (1st Edition Revision 1. This will expose the shield assembly for adjustment.
- STEP 3 Turn the APR-5000 power switch ON.
- STEP 4 Load and thread the work tape onto the machine.

STEP 5 Adjust the shield assembly dashpot for smooth operation of the shield assembly with the dashpot adjustment screw. Refer to Figure 6-7.

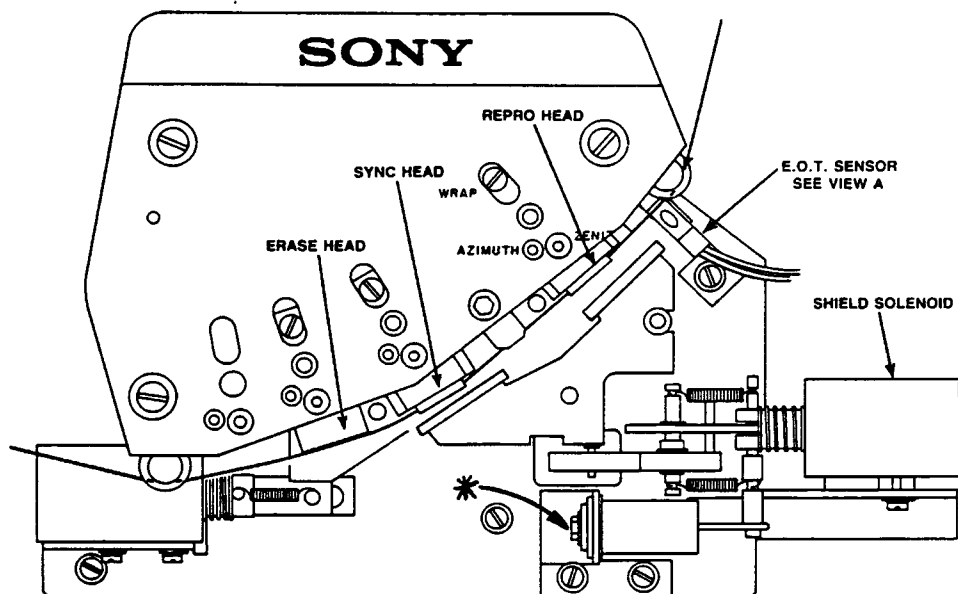


Figure 6-7. Shield Dashpot Adjustment

6.5.5 Reel Tach Sensor (RTS) Tape Tach Sensor (TTS) Check/Adjustment

Necessary Tools:

- Phillips Head Screwdriver
- Potentiometer Adjustment Tool (Tweaker)
- Oscilloscope
- Work Tape (7.5-inch reels required)
- 14-pin DIP Clip

Specification: 50% Duty Cycle for all signals

6.5.5.1 Tape Tachometer Sensor TTSA Check Procedure

The Reel Tach Sensors (RTS) and the Tape Tach Sensor (TTS) should be checked, and adjusted (if necessary) prior to performing adjustments on the tape tension or the Reel Motor Driver (RMD) offset adjustment. These adjustments cannot be properly done when the RTS or TTS are out of adjustment. In this procedure the output of the tachometer sensor circuits are set to have a 50% duty cycle. There are two signals being output from each RTS and TTS board (RTSA, RTSB or TTSA, TTSA). These signals are 90 degrees out of phase with respect to each other as a result of the physical dimensions of the IC. Note that when first attaching the oscilloscope probe to the test points (with the machine in STOP mode) a voltage of either +5vDC or 0vDC will be read on the

oscilloscope. This is normal due to the operation of the circuit. Actually the circuit of the RTS and TTS boards are indicating the position of a ferrous ring that is polarized North, South, North, South continually around its circumference. As a result, the arbitrary stopping point of a reel motor will yield either a +5vDC or 0vDC reading depending on which pole the sensor is being "read at the stop point (refer to Figure 6-8).

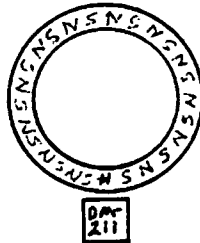


Figure 6-8. Ferrous Tachometer Ring

- STEP 1** Turn the APR-5000 power switch OFF.
- STEP 2** Open the Transport Control Panel.
- STEP 3** Connect the 14 pin DIP Clip to IC13 on the TIB board (refer to Figure 6-9).
- STEP 4** Turn the APR-5000 power switch ON.
- STEP 5** Load the work tape onto the machine.
- STEP 6** Press the PLAY key. This will place the machine into the PLAY mode.
- STEP 7** Connect the ground lead of the oscilloscope to TP1 of the TIB board. (Refer to Figure 6-9)
- STEP 8** Connect the positive lead of the oscilloscope to pin 8 of IC13 (via the DIP Clip). This is the TTSA signal. Set the oscilloscope uncalibrated sweep control so that one cycle of the waveform equals 10 horizontal segments (full scale) of the oscilloscope.

- STEP 3** Ensure that the duty cycle of the TTSB signal is 50%.
- STEP 4** If the duty cycle is not 50%, perform the adjustment procedure in Section 6.5.5.4 TTSB Adjustment Procedure.

6.5.5.4 Tape Tachometer TTSB Adjustment Procedure

- STEP 1** Perform the check procedure for the TTSB signal (Section 6.5.5.3).
- STEP 2** Adjust RV2 on the TTS board so that the TTSB signal at pin 10 of IC13 has a duty cycle of 50%.

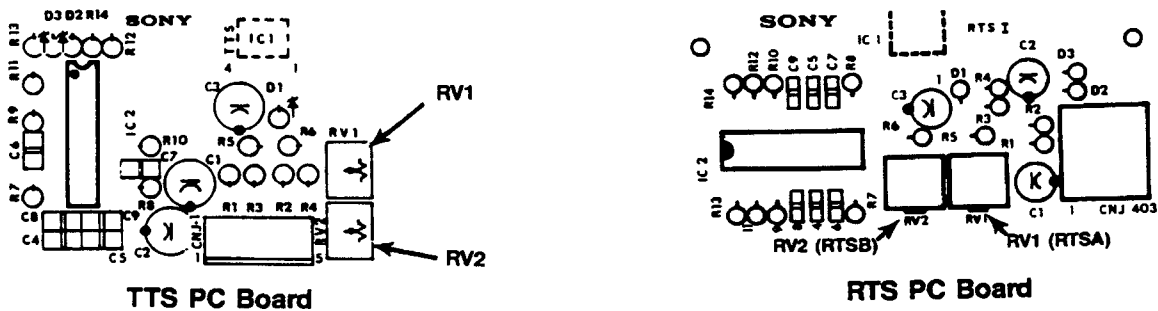


Figure 6-10. TTS/RTS Board Adjustment Potentiometers

6.5.5.5 Supply Reel Motor RTSA Check Procedure

- STEP 1** Proceed with Section 6.5.5.1 STEPs 1 through 6.
- STEP 2** Connect the 14-pin DIP Clip to IC13 on the TIB board. (refer to Figure 6-9)
- STEP 3** Connect the positive lead of the oscilloscope probe to IC13 pin 2 via the DIP Clip. This is the supply reel RTSA signal. Set the oscilloscope uncalibrated sweep so that one waveform equals ten horizontal segments (full scale).
- STEP 4** Ensure that the duty cycle of the supply reel RTSA signal is 50%. If the duty cycle is not 50% proceed to Section 6.5.5.6 Supply Reel Motor RTSA Adjustment Procedure.

6.5.5.6 Supply Reel Motor RTSA Adjustment Procedure

- STEP 1** Perform the check procedure for the supply reel motor RTSA signal (Section 6.5.5.5).
- STEP 2** Adjust RV1 on the supply RTS board so that the RTSA signal seen at pin 2 of IC13 has a duty cycle of 50%. (refer to Figure 6-10)

6.5.5.7 Supply Reel Motor RTSB Check Procedure

- STEP 1** Perform STEPS 1 through 6 of Section 6.6.5.1.
- STEP 2** Connect the 14-pin DIP Clip to IC13 on the TIB board. (Refer to Figure 6-9)
- STEP 3** Connect the positive lead of the oscilloscope probe to IC13 pin 4 via the DIP Clip. This is the supply reel RTSB signal. Adjust the uncalibrated sweep so that one cycle of the waveform equals ten horizontal segments (full scale).
- STEP 4** Ensure that the supply reel RTSB signal has a duty cycle of 50%. If the duty cycle is not 50%, proceed with Section 6.5.5.8 Supply Reel Motor RTSB Adjustment Procedure.

6.5.5.8 Supply Reel Motor RTSB Adjustment Procedure

- STEP 1** Perform the Supply Reel Motor RTSB Check Procedure (Section 6.5.5.7).
- STEP 2** Adjust RV2 on the supply reel RTS board so that the RTSB signal as seen at pin 4 of IC13 of the TIB board has a duty cycle of 50%. (refer to Figure 6-10)

6.5.5.9 Take-up Reel Motor RTSA Check Procedure

- STEP 1** Perform STEPS 1 through 6 of Section 6.5.5.1.
- STEP 2** Connect the 14-pin DIP Clip to IC13 of the TIB board. (refer to Figure 6-9)
- STEP 3** Connect the positive lead of the oscilloscope probe to IC13 pin 6 via the DIP Clip. This is the take-up reel motor RTSA signal. Adjust the uncalibrated sweep of the oscilloscope so that one cycle of the waveform equals ten horizontal segments (full scale).

STEP 4 Ensure that the take-up RTSA signal has a duty cycle of 50%. If the duty cycle does not equal 50%, perform the adjustment procedure in Section 6.5.5.10.

6.5.5.10 Take-up Reel Motor RTSA Adjustment Procedure

STEP 1 Perform the check procedure in Section 6.5.5.9.

STEP 2 Adjust RV1 on the take-up reel RTS board so that the take-up reel RTSA signal as seen at pin 6 of IC13 on the TIB board has a duty cycle of 50%. (refer to Figure 6-10)

6.5.5.11 Take-up Reel Motor RTSB Check Procedure

STEP 1 Proceed with STEPS 1 through 6 of Section 6.5.5.1.

STEP 2 Connect the 14-pin DIP clip to IC13 on the TIB board (refer to Figure 6-9).

STEP 3 Connect the positive lead of the oscilloscope probe to IC13 pin 12 via the DIP Clip. This is the take-up reel motor RTSB signal. Adjust the uncalibrated sweep of the oscilloscope so that one cycle of the waveform equals ten horizontal segments (full scale).

STEP 4 Ensure that the take-up reel motor RTSB signal has a duty cycle of 50%. If the duty cycle is not 50%, perform the adjustment procedure in Section 6.5.5.12.

6.5.5.12 Take-up Reel Motor RTSB Adjustment Procedure

STEP 1 Perform the check procedure in Section 6.5.5.11.

STEP 2 Adjust RV2 on the take-up reel RTS board (refer to Figure 6-10) so that the take-up RTSB signal seen at IC13 pin 12 (on the TIB board) has a duty cycle of 50%.

6.5.6 Reel Motor Driver (RMD) Check/Adjustment Procedure

- Necessary Tools:
- Digital Voltmeter
 - Alligator Clips (for connection of the voltmeter)
 - Potentiometer Adjustment Tool (tweezer)
 - Phillips Head Screwdriver
 - Work Tape
 - Tentelometer (T2-H12-2)
(Sony #J-6041-680-A)

Prerequisite: RTS/TTS Check/Adjustment

6.5.6.1 RMD Board DC Offset Check

The DC offset that the reel motor driver circuitry will have when the reel motors are in a NO TENSION mode must be adjusted to a minimum level for proper operation. This check/adjustment **MUST** be made before the check/adjustment of the RMD for tape tension.

STEP 1 Remove the screws on the upper rear door and open the door. This will expose the RMD board for adjustment. (Refer to Figure 6-11)

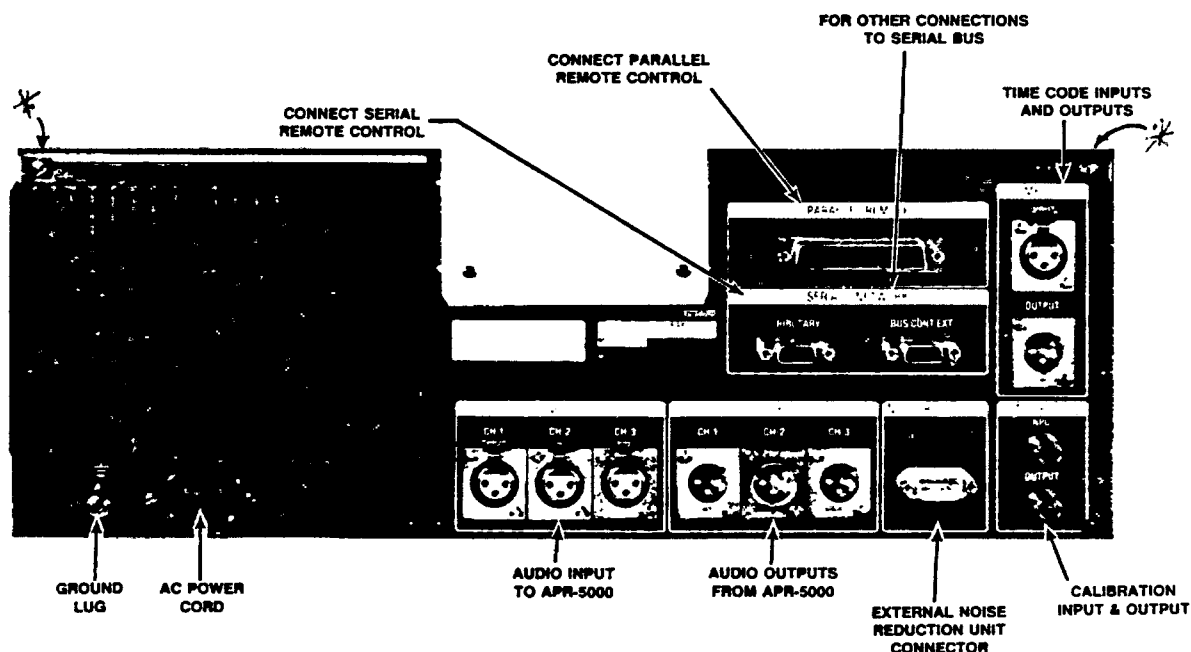


Figure 6-11. RMD Board Access

- STEP 2** Turn the APR-5000 power switch ON.
- STEP 3** Place a piece of tape (or other object) in the path of the EOT sensor. This will put the machine into IDLE mode (both reel motors will rotate slowly in opposite directions). Press the EDIT key once. This will put the machine into EDIT mode (both reel motors will stop rotation and there should be no tension applied).
- STEP 4** Connect the Digital Voltmeter to the RMD board as shown in Figure 6-12.
- STEP 5** Set the DVM to the millivolts scale and ensure a reading of +0.001 volts DC across R18. If this reading is not +0.001 volts DC, perform the adjustment procedure in section 6.5.6.2 STEP 1.
- STEP 6** Connect the DVM as shown in Figure 6-13.
- STEP 7** Set the DVM to the millivolts scale and ensure a reading of +0.001 volts DC across R17. If this reading is not +0.001 volts DC, perform the adjustment procedure in section 6.5.6.2 STEP 2.

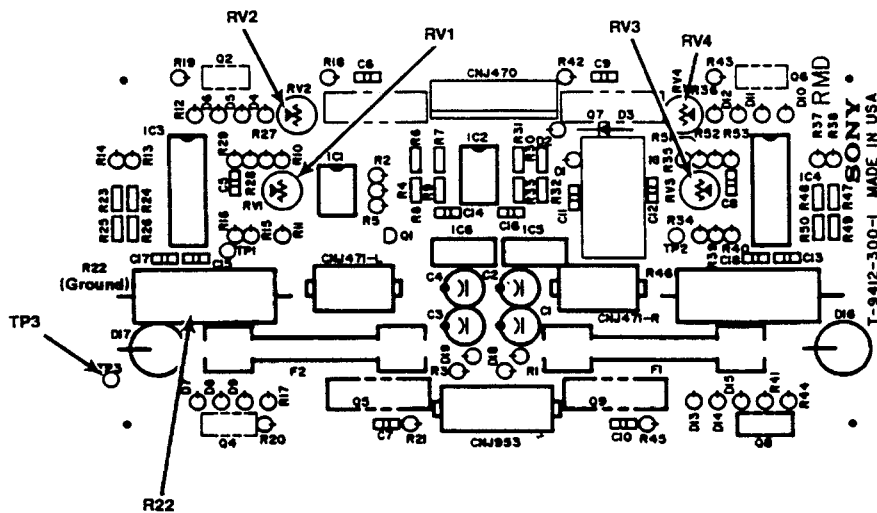


Figure 6-12. DVM Connection to the RMD Board

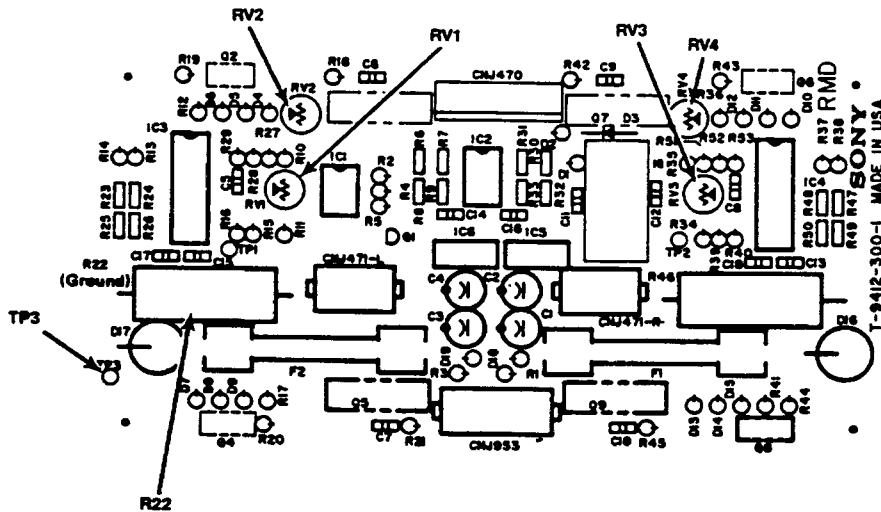


Figure 6-13. DVM Connection to the RMD Board

6.5.6.2 RMD DC Offset Adjustment Procedure

STEP 1 Adjust RV2 on the RMD board (refer to Figure 6-12) so that the voltage reading across R18 equals $+0.001$ volts DC. This adjustment must be made when the machine is in EDIT mode and no tension or reel motor rotation is occurring (refer to Figure 6-12 for DVM probe attachment points).

STEP 2 Adjust RV4 on the RMD board (refer to Figure 6-13) so that the voltage reading across R17 equals $+0.001$ volts DC. This adjustment must be made when the machine is in EDIT mode and no tension or reel motor rotation is occurring (refer to Figure 6-13 for DVM probe attachment points).

6.5.6.3 RMD Tension Check Procedure

The microprocessor controlled tape tension servo system feeds the tension data from a ROM table to the motor drive system. The physics of tape tension dictates that the torque on the reels necessary to maintain constant tape tension will vary as the amount of tape on the reels (tape mass radius) varies. The ROM table in the software of the APR-5000 is programmed to compensate for this.

Ultimately, this means that the microprocessor is providing the TIB board with the information necessary to maintain constant tension throughout the length of the tape. The TIB board converts this data along with a voltage fed back from the HES board into the DC control voltage that is then routed to the RMD board as the reel motor control voltage. The RMD board adjustments make the final determination of how the data (that originated at the CPU board) is interpreted into reel motor drive signals that ultimately control the tension of the tape.

STEP 1 Turn the APR-5000 power switch ON.

STEP 2 Load the work tape onto the machine.

STEP 3 Locate to the center of the tape mass (equal mass on both reels).

STEP 4 Press the PLAY key. This will put the tape machine in PLAY mode.

STEP 5 Check the supply side tension by placing the tentelometer at the supply side check point shown in Figure 6-14. The supply side tension in PLAY mode should equal 70g (+/-5g). If the supply side tension does not equal 70g (+/-5g), perform the adjustment procedure listed in Section 6.5.6.4.

STEP 6 Check the take-up side tension by placing the tentelometer at the take-up side check point as shown in Figure 6-14. The take-up side tension in PLAY mode should be 120g (+/-5g). If the take-up side tension is not 120g (+/-5g), perform the adjustment procedure shown in section 6.5.6.4.

STEP 7 Locate to a point near the end of the tape.

STEP 8 Repeat STEPs 5 and 6.

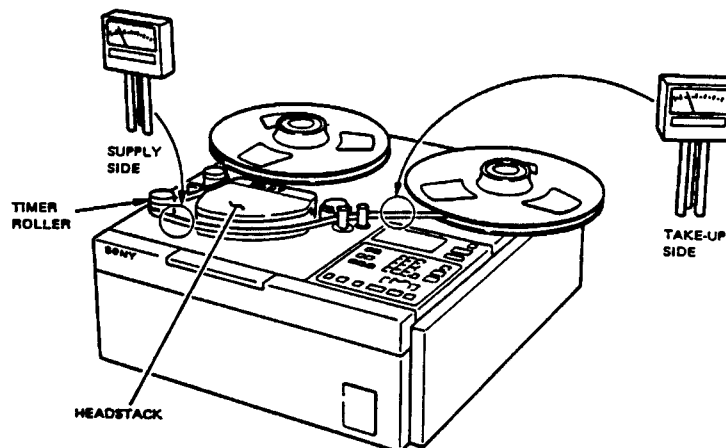


Figure 6-14. Tentelometer Placement

STEP 9 Locate to a point near the beginning of the tape.

STEP 10 Repeat STEPs 5 and 6.

****WARNING****

DO NOT CHANGE TAPE MOTION MODE WHILE TENTELOMETER IS IN TAPE PATH (i.e. PLAY mode to STOP mode), AS THIS WILL CAUSE DAMAGE TO THE MOVEMENT OF THE TENTELOMETER.

6.5.6.4 RMD Tension Adjustment Procedure

STEP 1 Proceed with Section 6.5.6.3 STEPs 1 through 4.

STEP 2 Remove the upper rear panel screws and lower the panel. This will expose the RMD board for adjustment.

STEP 3 Place the tentelometer at the supply side check point as shown in Figure 6-14.

STEP 4 Adjust RV1 on the RMD so that the reading on the tentelometer equals 70g (+/-5g). Refer to Figure 6-13 for potentiometer location.

STEP 5 With the machine still in PLAY mode, place the tentelometer at the take-up side check point as shown in Figure 6-14.

STEP 6 Adjust RV3 on the RMD board for a tentelometer reading of 120g (+/-5g). Refer to Figure 6-13 for potentiometer location.

Figure 6-15. (for future reference)

6.5.7 Flutter Dampener Arm Check/Adjustment

Necessary Tools: - Phillips Head Screwdriver
- Potentiometer Adjustment Tool (tweezer)
- Work Tape
- Digital Voltmeter

Prerequisite: - Complete Cleaning (Section 6.4)
- Tape Path Check/Adjustment
- RTS/TTS Check/Adjustment (Section 6.5.5)
- RMD Board Check/Adjustment (Section 6.5.6)

Specification:

- 1) TP-A (on the HES board) should exhibit equal positive and negative DC voltage values at both the extreme right side and extreme left side of flutter dampener arm travel. For example, if the extreme left side of flutter dampener arm travel renders a -5vDC value at TP-A, then the extreme right side of flutter dampener arm travel should render a value of +5vDC (+/-0.05vDC).
- 2) TP-B (on the HES board) should exhibit a 0.0vDC to +10.25vDC (+/-0.25vDC) voltage level variation when the flutter dampener arm is moved from the extreme right side to the extreme left side of flutter dampener arm travel. Hence, RV1 (on the HES board) adjusts this voltage level value, and RV2 (on the HES board) adjusts the "zero" point.

The Flutter Dampening Arm/Hall Effect Sensor (HES) board assembly rarely requires adjustment. More often than not, when the flutter dampener arm is not riding in the center of travel during PLAY mode, the tension adjustment of the RMD board is not set properly. Always check the tensions (and adjust if necessary) with a calibrated tentelometer BEFORE adjusting the Flutter Dampening Arm/Hall Effect Sensor (HES) board assembly.

STEP 1 Turn the APR-5000 power switch OFF. Remove any tape and/or reels from the unit. Remove the headstack assembly and the top front cosmetic cover. Replace the headstack assembly onto the unit.

STEP 2 Locate the HES board (directly under the Flutter Dampener Arm).

STEP 3 Connect the positive lead of the voltmeter to TPA on the HES board. Connect the negative lead to TP1 of the TIB board. Turn the APR-5000 power switch ON.

NOTE: A TIB board artwork modification (effective on rev #-?? and higher) changed the ground test point from TP2 to TP1. Refer to the PC board # on the TIB board for verification of specific artwork revision.

STEP 4 Move the Flutter Dampener Arm to the extreme right until the arm is in contact with the right side stopper. Ensure that a minimum reading of +5vDC exists.

NOTE: If the voltage values read in STEPS 4 and 5 do not exceed +/-5vDC, possibly one of the following components require replacement;

- Bar magnet (mounted on flutter dampener arm assembly)
- IC1 (Hall Effect Element on HES board)
- IC2 (differential amplifier stage on HES board)

STEP 5 Move the Flutter Dampener Arm to the extreme left until the arm is in contact with the left side stopper. Ensure that a minimum reading of -5vDC exists.

NOTE: The voltage values found in STEPS 4 and 5 will probably not be exactly +/-5vDC. Remember the parameter checked at TPA is not the absolute value of the two readings, but that the two voltages must be complementary (+5vDC to the right side and -5vDC to the left side +/-0.25vDC).

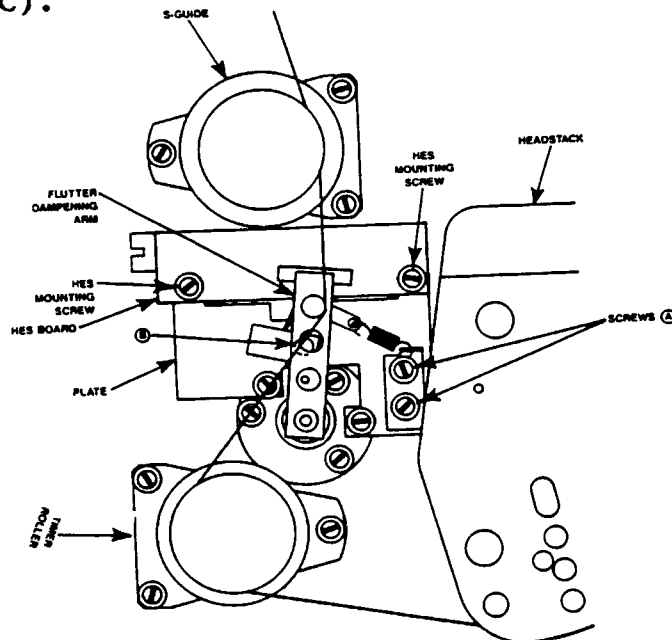


Figure 6-16. Flutter Dampening Arm Assembly

- STEP 6** If the voltage values read in STEPS 4 and 5 are not within specification ($\pm 0.25\text{vDC}$), this indicates that the hall effect sensor must be repositioned in the travel path of the magnet. This repositioning is accomplished by loosening the two securing screws on the HES board, and physically moving the HES board. Refer to Figure 6-16. Repeat STEPS 4 and 5 to check the readings at TPA and TPB.
- STEP 7** With the positive probe of the voltmeter connected to TPB (of the HES board), note the reading of the voltmeter as the flutter dampener arm is moved from the extreme right stopper to the extreme left stopper. The voltage value read on the meter should change 10.25vDC ($\pm 0.25\text{vDC}$). If the value is not within specification, adjust RV1 on the HES board to attain this reading.
- STEP 8** Load a work tape onto the machine.
- STEP 9** Place the machine into PLAY mode and ensure that the flutter dampener arm "rides" in the center of the end-to-end travel. If the flutter dampener arm does not meet this specification, loosen the screws (A) and adjust the spring tension. Refer to Figure 6-16.
- STEP 10** With the machine in PLAY mode, check the clearance of the stopper spring. There should be a clearance of 2-3mm between the lower flutter dampener shaft and the stopper spring during PLAY mode. If required, adjust the spring securing screw (B). Refer to Figure 6-17.

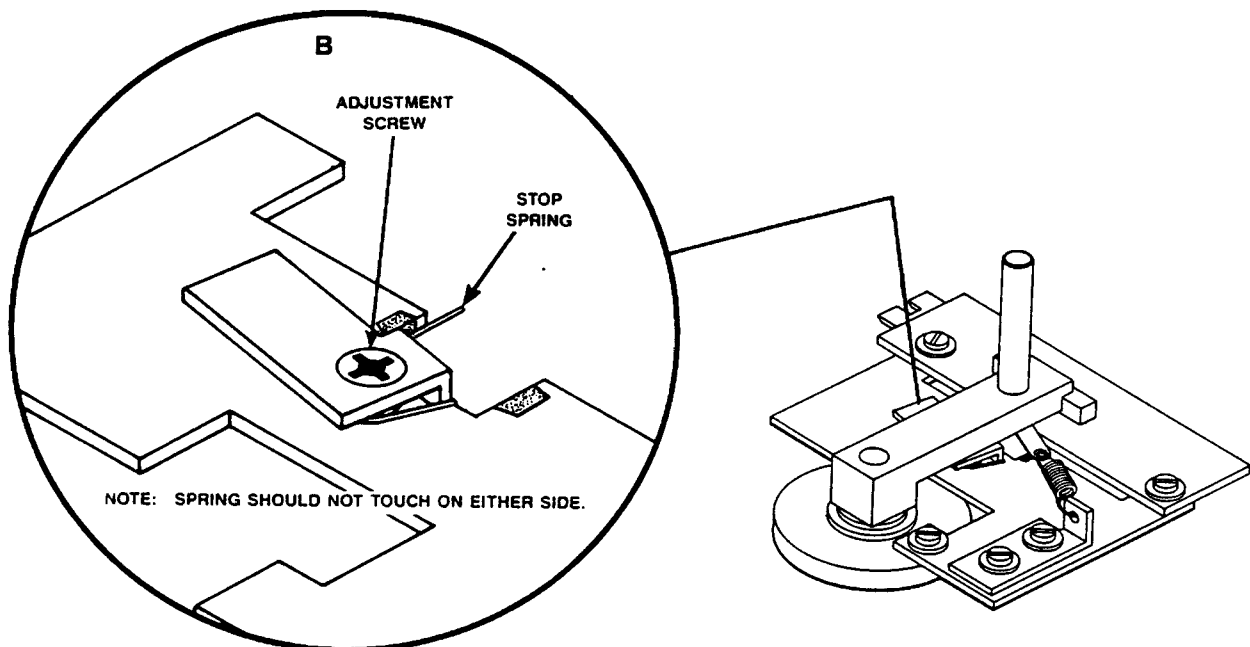


Figure 6-17. Flutter Dampener Stopper Spring Assembly

6.5.8 Flutter/Start-up Check/Adjustment

Necessary Tools: - Flutter Meter (EMT 424 or equivalent)
- Phillips Head Screwdriver
- Potentiometer Adjustment Tool (tweaker)
- Work Tape (in good condition for recording)

Prerequisite: - Complete Cleaning (Section 6.4)
- Tape Path Check/Adjustment
- RTS/TTS Check/Adjustment (Section 6.5.5)
- RMD-II Check/Adjustment (Section 6.5.6)
- Flutter Dampener Check/Adjustment (Section 6.5.7)

Flutter

Specification: - 30ips: 0.025% DIN 45507 Weighted
- 15ips: 0.035% DIN 45507 Weighted
- 7.5ips: 0.055% DIN 45507 Weighted
- 3.75ips: 0.100% DIN 45507 Weighted

Start-up

Specification: - 30ips: 1600msec to .3% flutter DIN 45507 Weighted
- 15ips: 800msec to .3% flutter DIN 45507 Weighted

The flutter specification (or jitter content) on any tape recording machine is of great importance to the quality of the recordings the machine will produce. The APR-5000 utilizes a Capstan Servo Loop (CSL) system to alleviate the inherent flutter that are a part of all tape recording machines. The flutter adjustment does not need to be performed at regular service intervals. Once the flutter adjustment is set at the factory, it will only need adjustment when one of the components of the capstan servo loop are repaired or replaced (i.e. capstan motor, CSL board, or a component thereof).

6.5.8.1 Flutter/Start-up Check Procedure

- STEP 1** Turn the APR-5000 power switch ON.
- STEP 2** Load the work tape.
- STEP 3** Connect the flutter meter to the APR-5000. The output of the flutter meter will connect to any one of the LINE INPUT connectors on the APR-5000. The input of the flutter meter will be connected to the LINE OUTPUT of the channel chosen, for example, connect to the LINE INPUT and the LINE OUTPUT of channel 15.
- STEP 4** Set up the APR-5000 in the following way:
- Select REPRO Mode on the Meter Bridge
 - Select All Channels to RECORD READY Mode
 - Select 30ips (HI Speed)
 - Select RECORD Mode by pressing the PLAY and RECORD Buttons Simultaneously
- STEP 5** Observe the flutter meter reading. The flutter reading should be less than 0.025% @ 30ips, (and less than 0.055% @ 7.5ips). If the reading on the flutter meter is greater than the specification, perform the adjustment procedure in Section 6.5.8.2.
- STEP 6** Set the Flutter meter to start-up check mode. Ensure the start-up specification of 900msec @ 30ips is attained.
- STEP 7** Change tape speed to 15ips (MID Speed), place machine into RECORD mode (as shown in STEP 4) and observe the flutter meter reading of less than 0.035% @ 15ips. If the reading on the flutter meter is greater than the specification, perform the adjustment procedure in Section 6.5.8.2.
- STEP 8** Check the start-up reading of 500msec @ 15ips.

NOTE: When adjusting the flutter of the APR-5000 note that the optimum flutter position of RV2 (on the CSL board) may not be the optimum position for meeting the start-up specification. Hence, if an adjustment is made to improve flutter, be sure to check the start-up specification after adjustment is made.

STEP 9 Change tape speed to 7.5ips (LO Speed), place machine into RECORD mode (as shown in STEP 4) and observe the flutter meter reading of less than 0.055% @ 7.5ips. If the reading on the flutter meter is greater than the specification, perform the adjustment procedure in Section 6.5.8.2.

STEP 8 Check the start-up reading of 500msec @ 7.5ips.

NOTE: When adjusting the flutter of the APR-5000 note that the optimum flutter position of RV1 (on the CSL board) may not be the optimum position for meeting the start-up specification. Hence, if an adjustment is made to improve flutter, be sure to check the start-up specification after adjustment is made.

6.5.8.2 Flutter/Start-up Adjustment Procedure

STEP 1 Perform STEPs 1 through 4 of Section 6.5.8.1.

STEP 2 Open the ALN panel door and remove the two securing screws of the power supply access door panel and open the panel to expose the CSL board (refer to Figure 6-18).

STEP 3 Locate and adjust RV1 (for 7.5ips and 3.75ips) and/or RV2 (for 30ips and 15ips) to meet the specification.

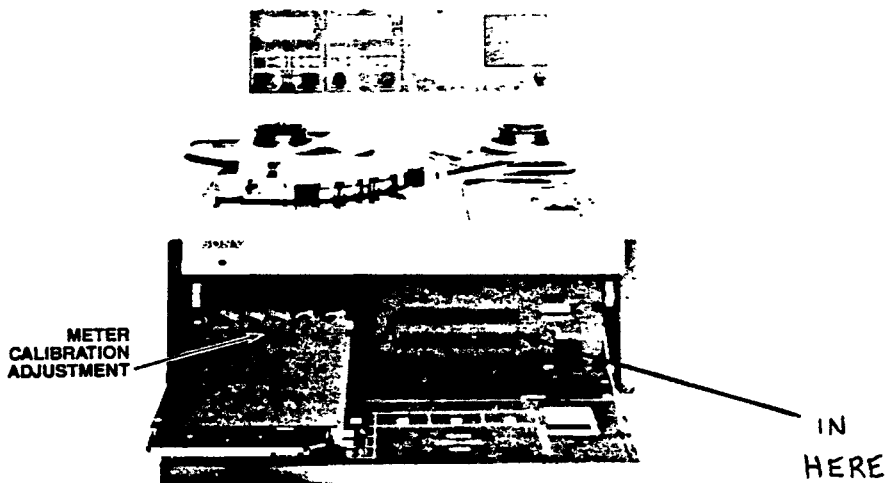


Figure 6-18. CSL Board Access

6.5.9 End Of Tape (EOT) Sensor Check/Adjustment

Necessary Tools: - Phillips Head Screwdriver
- Work Tape
- Potentiometer Adjustment Tool (tweaker)

Prerequisite: - NONE

Specification: - As Necessary (user discretion)

The sensitivity adjustment of the EOT sensor is set at the user's discretion. Since the APR-5000 encounters varying lighting environments, the requirements of each individual machine EOT sensor sensitivity adjustment cannot be standardized. The following check/adjustment procedures are given as a guide in the event of EOT sensor element replacement or if there is a desire to change the sensitivity for adverse (or varying) light conditions (such as camera flash bulbs, film studio lighting, etc.). The EOT sensor circuit is physically mounted on the KBD board.

6.5.9.1 EOT Sensor Check Procedure

STEP 1 Turn the APR-5000 power switch ON.

STEP 2 Load the work tape onto the machine.

STEP 3 With the transport in STOP mode, check the physical gap between the tape and the EOT sensor. The tape should not touch the EOT sensor.

STEP 4 Move the tape in and out of the EOT sensor beam path and ensure that the APR-5000 enters STOP mode when the tape breaks the beam, and NO TAPE (absence of tape tension) mode when the tape is not breaking the beam. If the EOT sensor is not operating in this manner, or it is desired to change the sensitivity perform the adjustment procedure in Section 6.5.9.2.

6.5.9.2 EOT Adjustment Procedure

STEP 1 Turn the APR-5000 power switch OFF.

STEP 2 Remove any tape from the machine. Remove the two securing screws from the rear side of the top rear cosmetic panel and remove the panel. This will expose the two securing screws for the KBD assembly. Remove the two KBD securing screws and carefully lift the KBD/DSP assembly up. This will expose RV2 on the KBD board for adjustment. Place a non conductive material (cardboard, thick paper, etc.) between the KBD/DSP assembly and the CPU board and rest the KBD/DSP assembly on this material. Refer to the drawing shown in Figure 6-19.

STEP 3 Load the work tape onto the machine.

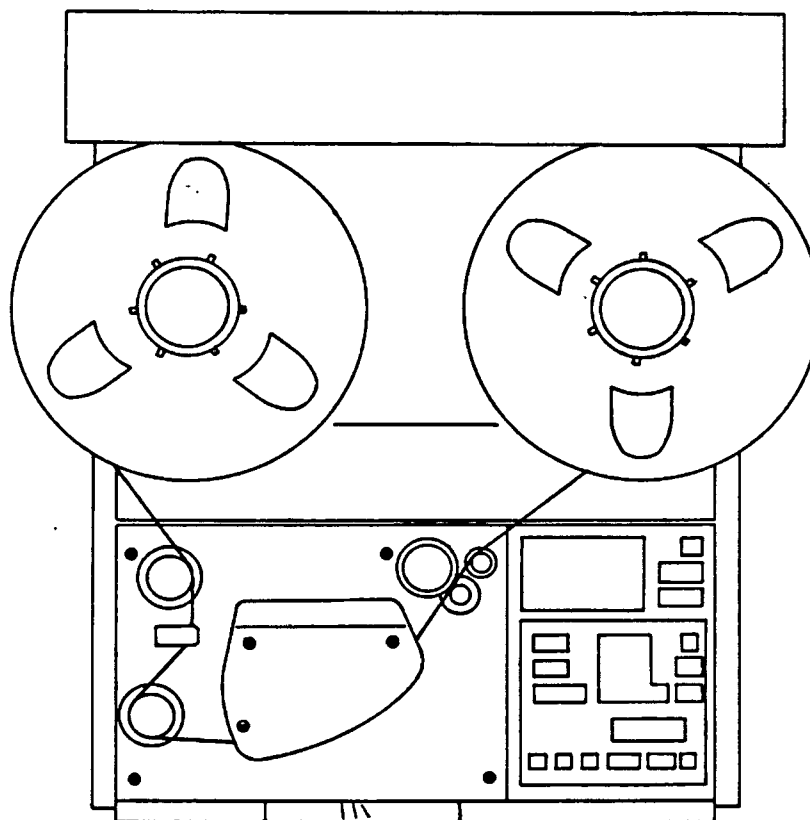


Figure 6-19. KBD Board Access

STEP 4 Adjust RV2 on the KBD board for desired EOT sensor sensitivity (refer to Figure 6-20).

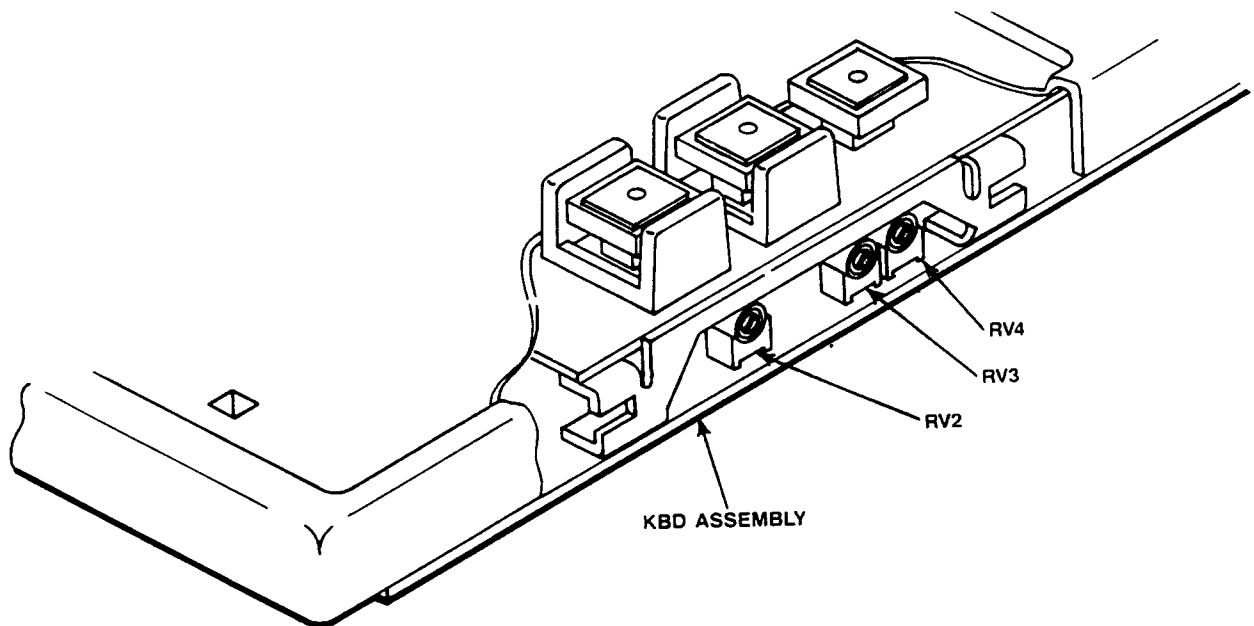


Figure 6-20. EOT Sensitivity Adjustment Location

6.5.10 Variable Speed Check/Adjustment Procedure

- Necessary Tools:**
- MRL Test Tape (or equivalent)
 - Work Tape
 - Phillips Head Screwdriver
 - Potentiometer Adjustment Tool (tweezer)
 - Frequency Counter
 - Digital Voltmeter (DVM)
 - 14 pin DIP Clip

- Prerequisites:**
- RTS/TTS Check/Adjustment
 - RMD Check/Adjustment
 - Flutter/Start-up Check/Adjustment

- Specification:**
- Reference Voltage at TP3 (TIB) -10.24vDC
 - IC24 pin 7: Test Mode 1.....14.4kHz
 - Test Mode 2.....28.8kHz

The variable speed adjustment is provided for two reasons. First, it will center the range of the vari-speed play speeds. This adjustment ensures a vari-speed range that is equal magnitude in each direction away from the standard speed. This means that the entire range from +50% of standard speed to -50% of standard speed is available. Second, this adjustment ensures the accuracy of the percentage of deviation reading displayed in the LOCATE TIME display to the actual tape speed.

This adjustment rarely needs to be performed and generally is only done when there have been electrical parts changes in the capstan drive circuit.

6.5.10.1 Variable Speed Check Procedure

- STEP 1** Turn the APR-5000 power switch ON.
- STEP 2** Load the MRL reference tape onto the machine. Make sure that all channels are in SAFE mode. Locate to the 1kHz tone. Make sure that the correct speed is selected on the APR-5000. For this check it is inconsequential which speed is selected. If there is a misadjustment, it will be evident in all speeds.
- STEP 3** Connect the frequency counter to the LINE OUT of either channel one or channel two.
- STEP 4** Play the 1kHz tone at standard speed (either 7.5ips, 15ips or 30ips). Ensure that there is a 1kHz reading on the frequency counter.
- STEP 5** Press the VARI key so that the key flashes. Press 5, 0, 0, on the ten-key pad. Press the VARI key once more so that the VARI key is constantly illuminated. The machine is now in VARI-SPEED PLAY mode +50% of standard speed.
- STEP 6** Ensure that the reading on the frequency counter is 1.5kHz. If the frequency counter shows a reading other than 1.5kHz, perform the adjustment procedure in section 6.5.10.2.
- STEP 7** Press the VARI key twice so that it flashes. Press the +/- key (on the ten-key pad) once. The display should read "-50.0". Press the VARI key once more so that the VARI key is constantly illuminated. The machine is now in VARI-SPEED PLAY mode -50% of standard speed.
- STEP 8** Ensure that the reading on the frequency counter is 500Hz. If the frequency counter shows a reading other than 500Hz, perform the adjustment procedure in section 6.5.10.2.

6.5.10.2 Variable Speed Adjustment Procedure

- STEP 1** Remove the top rear (deck plate) cosmetic cover exposing the TIB board.
- STEP 2** Load the work tape onto the machine.
- STEP 3** Connect the negative probe of the DVM to TP1 on the TIB board. (Refer to Figure 6-21)
- STEP 4** Connect the positive probe to TP3 on the TIB board. (Refer to Figure 6-21)

STEP 5 Adjust RV1 (on the TIB board) so that the voltage at TP3 equals -10.24VDC .

STEP 6 Turn the APR-5000 power switch OFF and disconnect the blue jumper block JU-1 (refer to Figure 6-21) on the TIB board.

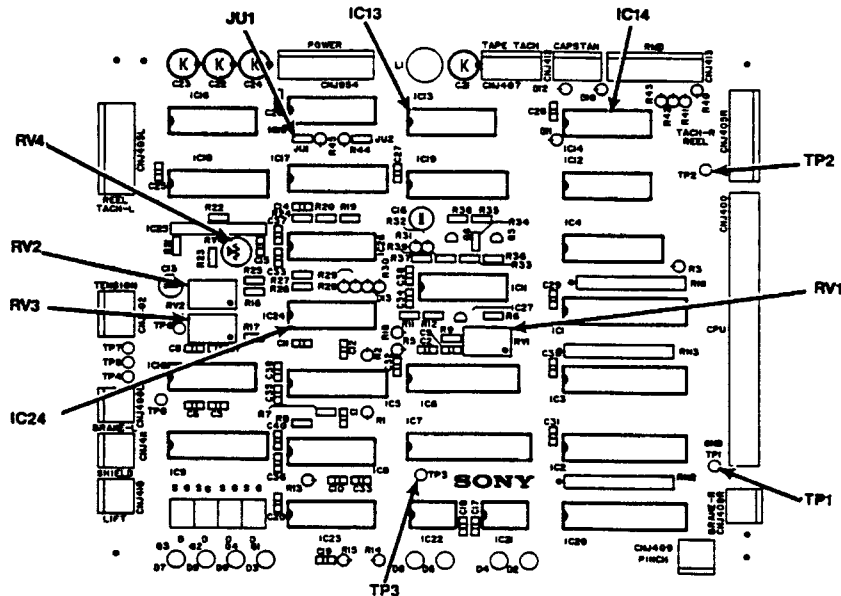


Figure 6-21. TIB Board Layout

STEP 7 Turn the APR-5000 power switch ON.

STEP 8 Press the STOP key once. This will place the machine into TIB test mode 1.

STEP 9 Connect the 14 pin DIP Clip to IC24 on the TIB board (Refer to Figure 6-21).

STEP 10 Connect the frequency counter probe to pin 7 of IC24 on the TIB via the DIP Clip. Adjust RV2 on the TIB board for a reading of 14.4kHz.

STEP 11 Press the STOP key again. This will place the machine into test mode 2.

STEP 12 Adjust RV3 on the TIB board so that the reading on the frequency counter (at pin 7 of IC24) is 28.8kHz.

STEP 13 Turn the power switch OFF and replace JU-1 back in its original position (Refer to Figure 6-21).

STEP 14 Verify the adjustments by performing the check procedure in section 6.5.10.1.

6.6 Audio System Check/Adjustment Procedures

This section contains all check/adjustment procedures for a complete audio system alignment of the **APR-5000** Analog Recorder. To ensure optimum results from the audio system adjustment procedures the following prerequisites are necessary:

- All test equipment is in good working order and recently calibrated.
- The **APR-5000** transport performance and mechanical alignments have been verified.
- All test tapes are in good condition.

These basic checks are quite important as all audio adjustment references rely on the accuracy of these prerequisite adjustments.

In adjusting the **APR-5000** audio system, there are seven major areas to cover:

- Head Alignment Check/Adjustment
- Input Calibration Check/Adjustment
- Meter Calibration Check/Adjustment
- Playback Calibration Check/Adjustment
- Record Calibration Check/Adjustment
- Secondary Record Compensation Check/Adjustment
- Bias and Erase Check/Adjustment

These areas are covered completely in the check/adjustment procedures to follow. The order in which the check/adjustment procedures are listed will facilitate optimum results. As in all tape recorders, some of the alignments require prerequisite check/adjustments to be made, since the later check/adjustment procedures rely on the accuracy of the preceding adjustments. The **APR-5000** audio alignments are quite stable. Hence, the accuracy is maintained until there is a desire to implement a change (i.e. different tape formulation, new headstack, different reference fluxivity, etc.). As in the transport check/adjustment procedures, if there is a part replaced in the audio circuitry, the check/adjustment procedures that are directly effected by the component change should be performed. This is done to verify the performance of the new component and to ensure its alignment to the specific machine.

The APR-5000 was designed with the service engineer in mind. The connections for the necessary test equipment are provided on the rear panel of the machine. The test equipment is connected as shown in Figure 6-22. As shown in this drawing, the CALibration INput (CAL IN) and CALibration OUTput (CAL OUT) connectors can be connected to permanent lines of the test equipment. Utilizing the calibration input and output connectors not only simplifies the connections, they also provide an accurate distribution amplifier on the input side and an accurate combining network on the output side. When performing the azimuth check/adjustment procedures the output of the CAL OUT connector is a summed output of all audio channels. This will provide the signal necessary to adjust the azimuth to the correct peak.

Utilizing the CAL IN and CAL OUT connectors also provides ease in channel switching when aligning channels individually.

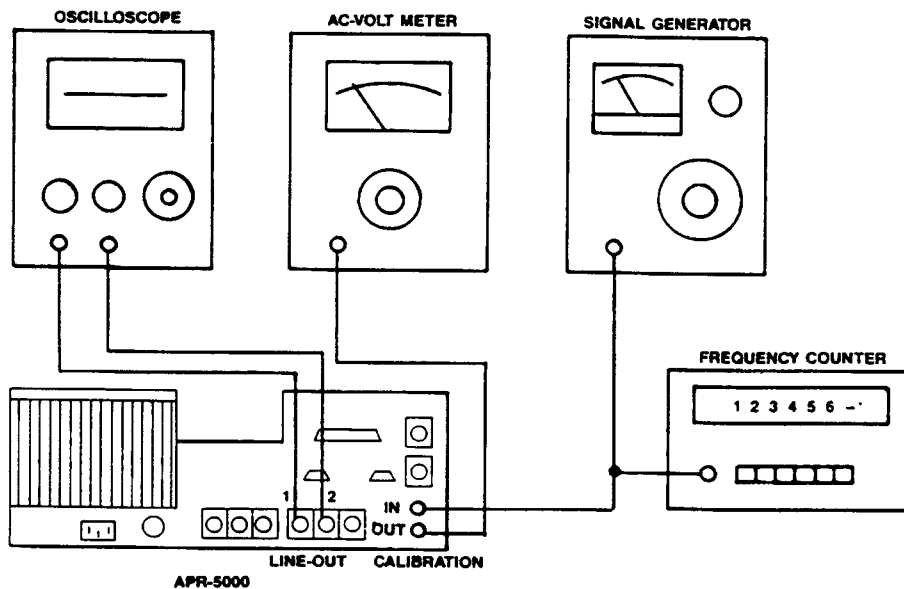


Figure 6-22. Connection of Test Equipment

6.6.1 Head Azimuth and Wrap Check/Adjustment Procedure

Necessary Tools: - MRL Test Tape (or equivalent)
- Flat Blade Screwdriver
- ACVM (HP 400 FL or equivalent)
- Oscilloscope
- 2mm Hex Allen Driver

Prerequisites: - Mechanical Headstack Check/Adjustment

Specification: - All channels will be in phase (zero phase difference) by azimuth adjustment.
- The reproduced level of all channels on each head are maximized by the wrap adjustment

In Section 6.5, procedures were given to adjust the heads in relationship to the tape path (head height and head zenith). The following procedures are given for the check/adjustment of the head wrap and head azimuth referring to the electrical signal output from the heads. These fine adjustments should not affect the tape path across the headstack yet will perform the optimization of the audio response of the heads in regard to playback levels and phase relationship.

Azimuth adjustments are especially important. If the head gaps are not all parallel to the direction the tape is traveling, segments of the same recorded wavelength will enter and leave each gap at different increments of time. The head azimuth adjustment performs the fine adjustment of the phase relationship between all channels of the multitrack head. This adjustment is set so that there is minimum phase difference between all channels.

The head wrap adjustment is an eccentric mounting screw which controls the position of the head gap in relationship to the tape which is entering or leaving the head surface. The audio playback level peaks (achieves maximum amplitude) when the gap is located in the exact center of the angle at which the tape touches the head an equal distance on each side of the head gap.

These adjustments are not necessary unless the tape path has been changed or adjusted due to the replacement of a worn component, or the installation of a new headstack. If the headstack is being replaced, refer to Section 6.3.1.

6.6.1.1 Head Wrap and Azimuth Check Procedure

STEP 1 Turn the APR-5000 power switch ON.

STEP 2 Connect the test equipment (Oscilloscope and ACVM) as shown in Figure 6-22.

STEP 3 Select HI speed and load the test tape onto the machine. Ensure that all channels are in SAFE mode. **DO NOT RECORD ON THE TEST TAPE.**

STEP 4 Press the REPRO keys for each channel on the Meter Bridge. This will place the selected channels of the machine into REPRO mode (reading signals from the tape via the Repro head).

STEP 5 Locate to the 10kHz tone on the test tape.

NOTE: When using the MRL test tapes (either 30ips, 15ips or 7.5ips) the 1kHz tone and the 10kHz tone can be accessed easily and quickly by using the following method.

STEP 1 Load the MRL test tape (tails out) and keystroke 15min 30sec into the tape time display. Remember that the APR-5000 displays must not be in TC mode.

STEP 2 Clear the LOCATE display, and enter 5min 46sec into the LOCATE display.

STEP 3 Press the LOCATE key. This will locate the machine to the approximate begin point of the 10kHz tone. The 1kHz tone is located by clearing the LOCATE display and pressing the LOCATE key.

STEP 6 Press the PLAY key.

STEP 7 Observe the phase relationship of channel 1 to channel 2. After observing the waveform phase relationship, observe the ACVM reading. Check the wrap adjustment by adjusting the wrap adjustment screw (Refer to Figure 6-26) clockwise then counter-clockwise. If there is a phase difference or the amplitude of the signal at the ACVM increases as a result of turning the wrap screw, perform the adjustment procedure in Section 6.6.1.2.

STEP 8 Repeat STEPs 1 through 7 for the Sync head.

6.6.1.2 Head Wrap and Azimuth Adjustment Procedure

NOTE: The following procedure is used for both the Repro head and the Sync head. When adjusting the head stack, be sure to adjust both the Repro head and Sync head.

- STEP 1** Press the ALL key on the ALN panel. This will provide the sum of all 2 channels as the output of the CAL OUT connector.
- STEP 2** After having completed the check procedure in Section 6.6.1.1, continue with the wrap adjustment. The wrap adjustment screw should be rotated to find the peak reading on the ACVM. Remember to attain a reading on the ACVM the machine must be playing back the test tape (as in Section 6.6.1.1).
- STEP 3** While playing back the 10kHz tone, adjust the azimuth adjustment screw (Refer to Figure 6-23) so that the reading on the ACVM is at peak amplitude. When the peak amplitude of the ACVM is read, check the phase relationship of the signals on the oscilloscope. All channels will be in phase.

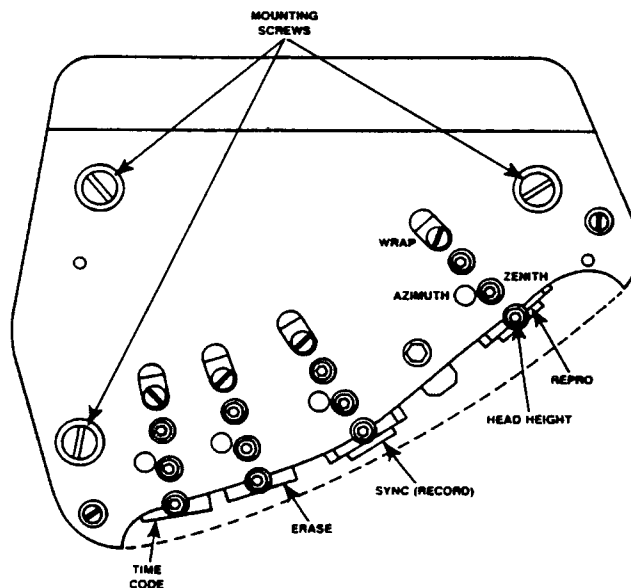


Figure 6-23. Headstack Adjustment Screw Locations

6.6.2 Input Level Check/Adjustment

Necessary Tools: - Frequency Generator
- Oscilloscope
- ACVM
- Frequency Counter

Prerequisite: - NONE

Specification: - Input level equals output level in INPUT mode (+4dBm).

The INPUT mode level check/adjustment is performed in the event that the INPUT mode level is questioned. Normally this adjustment rarely needs to be performed. In the case of changed components in the input circuit, this check/adjustment procedure is mandatory to ensure proper alignment of the circuitry with the new component(s) installed.

6.6.2.1 Input Level Check Procedure

STEP 1 Turn the APR-5000 power switch OFF.

STEP 2 Connect the test equipment as shown in Figure 6-22.

STEP 3 Turn the APR-5000 power switch ON.

STEP 4 Set the frequency generator to inject a +4dBm 1kHz sine wave into the calibration input.

STEP 5 Expose the ALN Panel as shown in Figure 6-24.

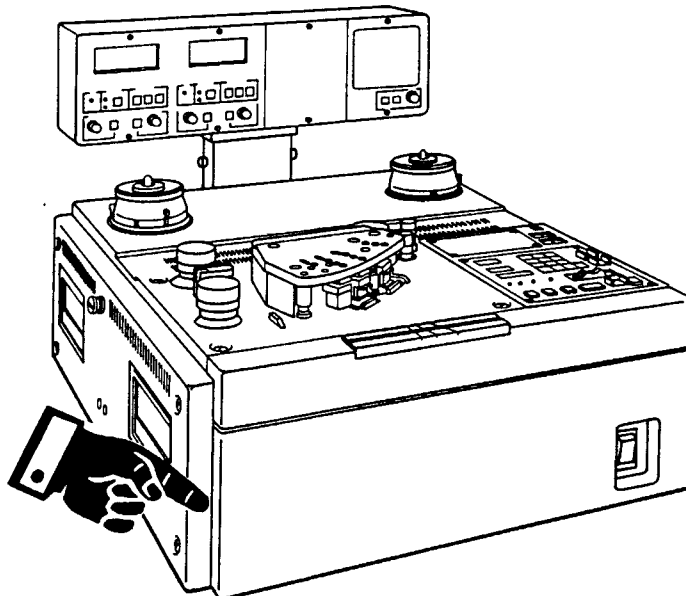


Figure 6-24. ALN Panel Location

STEP 6 Press the IND key once, refer to Figure 6-25. The IND key will illuminate, and a 1 will appear in the STATUS display of the ALN Panel.

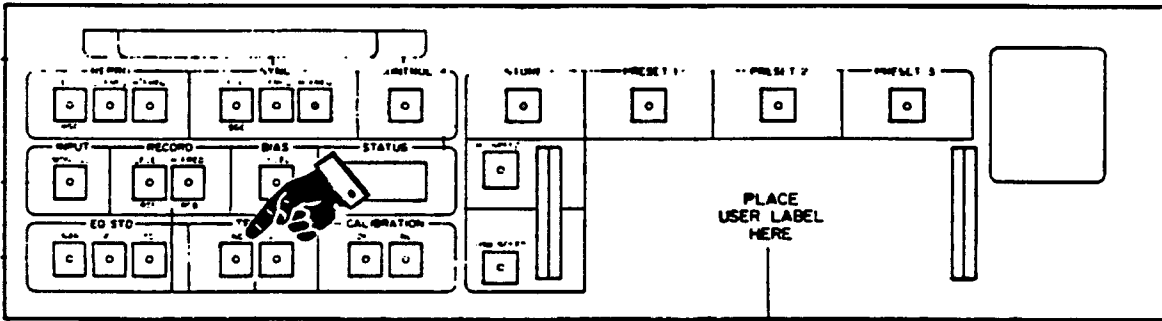


Figure 6-25. IND Key Location

NOTE: Along with these indicators, the meter panel will indicate that channel 1 has been selected for alignment. This is signified by a 1 appearing in the STATUS display and the ALN indicator illuminating on the STATUS display of the Meter Bridge. Refer to Figure 6-26.

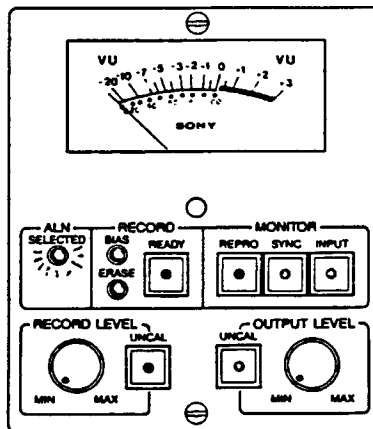


Figure 6-26. Meter Panel (Channel 1 ALN Selected)

STEP 7 Press the MON LVL key located in the INPUT section of the ALN Panel (Refer to Figure 6-27).

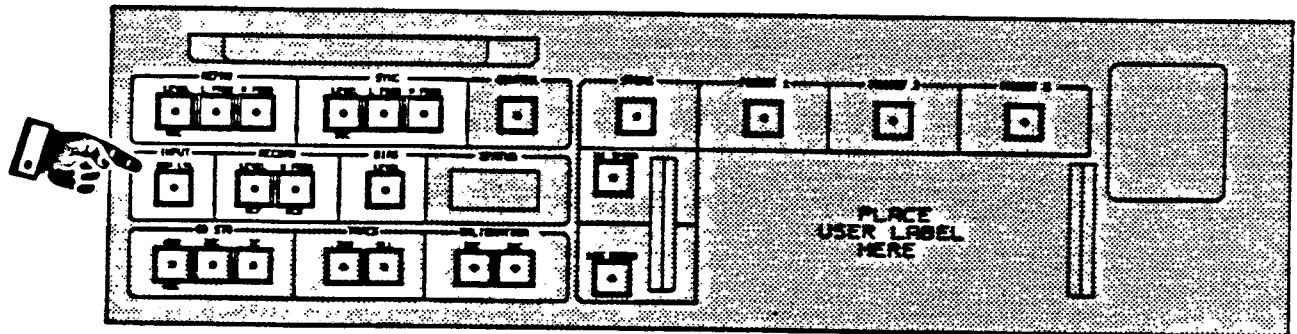


Figure 6-27. MON LVL Key Location

NOTE: By pressing the MON LVL key, INPUT mode is selected on the channel 1 CNL card. This mode is verified by the MON LVL key illuminating, the STATUS display of the ALN Panel displaying an alpha-numeric symbol (Hexi-decimal), the VU meter displaying signal level readings and the INPUT LED illuminating on the meter panel. Refer to Figure 6-28.

STEP 8 Check the reading on the ACVM. This is the input level of channel 1. This signal level should be +4dBm +/- 0.2dBm.

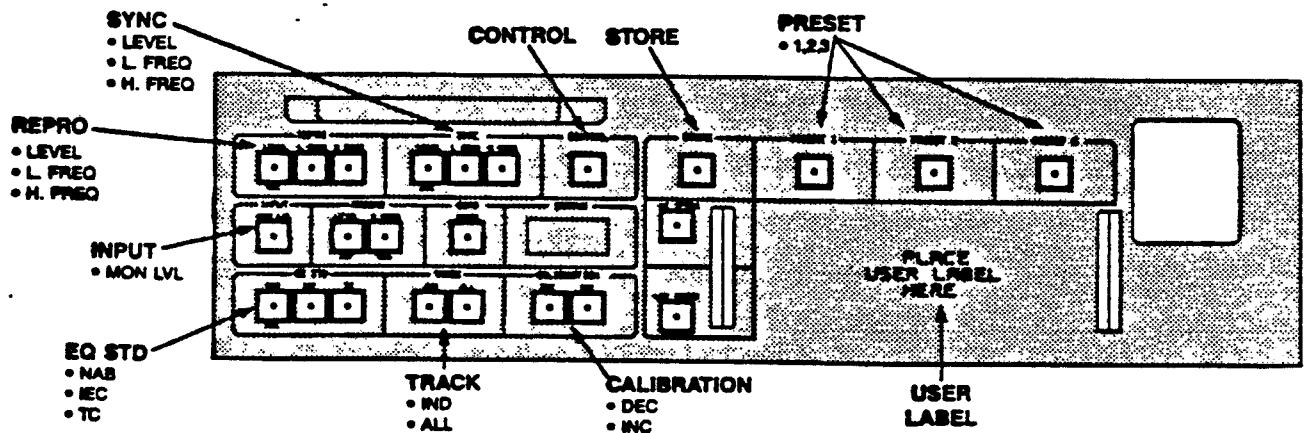


Figure 6-28. Channel 1 MON LVL ALN Indicators

STEP 9 If the signal level is not +4dBm, perform the adjustment procedure in Section 6.6.2.2. Repeat STEPS 8 and 9 for the remaining channels. To access the next channel, press the IND key. Holding the CONTROL key down while pressing the IND key will allow decent of channel number (i.e. 2, 1, etc.).

6.6.2.2 Input Level Adjustment Procedure

STEP 1 After performing STEPS 1 through 9 of Section 6.6.2.1, manipulate the INC and/or DEC keys in the CALIBRATION section of the ALN Panel to adjust the INPUT signal level. For this adjustment, utilize the same test equipment connection shown in Figure 6-22. Refer to Figure 6-29.

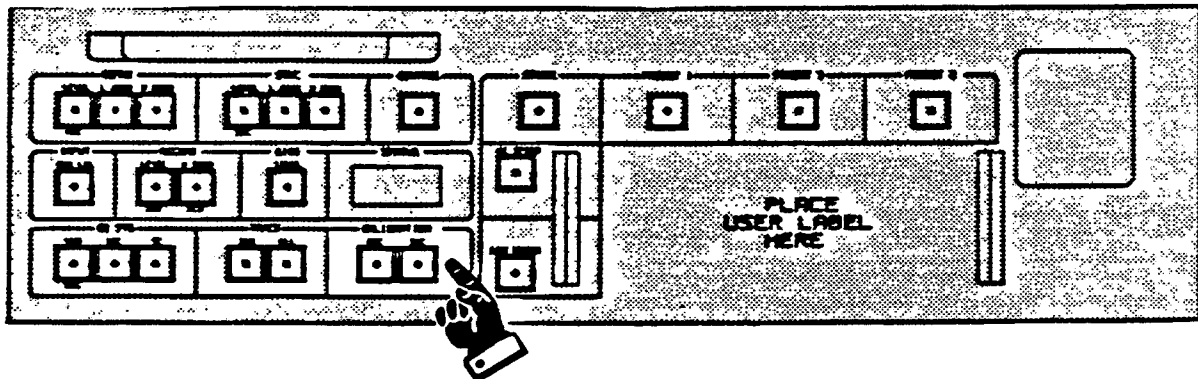


Figure 6-29. INC & DEC Key Location

STEP 2 Repeat STEP 1 for other channels that are in need of alignment. For access to the next channel, refer to Section 6.6.2.1, STEP 9.

6.6.3 Meter Calibration Check/Adjustment Procedure

Necessary Tools: - Frequency Generator
- Oscilloscope
- ACVM
- Frequency Counter
- Phillips Head Screwdriver
- Potentiometer Adjustment Tool (tweaker)
- Mirror (optional)

Prerequisite: - Input Calibration Check/Adjustment

Specification: - All meters will read 0VU with a +4dBm signal input

Although it is not required that the Meter Calibration check/adjustment procedure be done at regular service intervals, there may be a need to perform this procedure in the event of a meter or other component replacement. Since almost all studio repro and record alignments are done utilizing the meters on the machine itself, the accuracy must be exacting. The metering circuitry for the APR-5000 is designed for minimum drift with all components closely matched. The APR-5000 CNL card has three separate outputs. These are the differential line out, meter out, and the cal sum buss. The differential line out is fed to the XLR connectors on the back of the machine. The meter buffer (IC9 on CNL) output is routed to the VU meters and has a separate adjustment on the CNL card. The cal sum buss is routed to the calibration output on the rear panel of the machine. The VU meters will respond to the recorded signal, not the output signal of the machine. For this reason, it is advisable to re-align the meters during installation, to compensate for load impedance variations in consoles and outboard equipment of the specific installation.

6.6.3.1 Meter Calibration Check Procedure

STEP 1 Turn the APR-5000 power switch OFF.

STEP 2 Connect the test equipment as shown in Figure 6-22.

STEP 3 Turn the APR-5000 power switch ON.

STEP 4 Press the INPUT keys for each channel on the meter bridge. This will place all channels in INPUT mode.

STEP 5 Set the frequency generator to inject a +4dBm 1kHz sine wave into the CAL IN connector.

STEP 6 Ensure that with the +4dBm 1kHz sine wave signal input to the machine, the VU meters read 0VU. Refer to Figure 6-30.

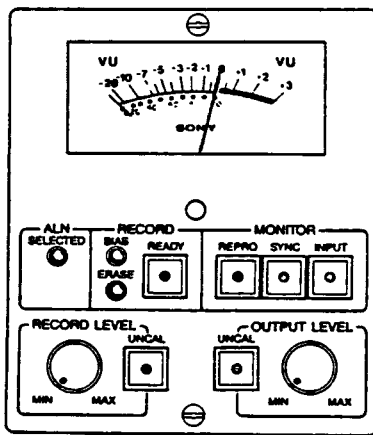


Figure 6-30. Reading for 0VU

STEP 7 If the VU meter(s) is(are) not reading 0VU, perform the adjustment procedure in Section 6.6.3.2.

6.6.3.2 Meter Calibration Adjustment Procedure

- STEP 1** Inject a +4db, 1khz sine wave to all channels (line in).
- STEP 2** With the operating load connected, connect the AC voltmeter to the line output of channel #1.
- STEP 3** Adjust the input level of channel #1 (on the ALN panel), for +4db, on the AC voltmeter.
- STEP 4** Repeat steps 2 and 3 for channel #2.
- STEP 5** Store these parameters in preset #1. This is done by pressing and holding the CONTROL key on the ALN panel, and while holding the CONTROL key down press the STORE key (also on the ALN panel). This action will cause the STORE key to illuminate. While the STORE key is illuminated, press the PRESET 1 key. The storage is complete.
- STEP 6** Turn the APR-5000 OFF.
- STEP 7** Install CNL #1 on an extender card and insert into CNL slot #1.
- STEP 8** Turn the APR-5000 ON.
- STEP 9** Adjust RV3 on the CNL for 0VU on the CH-1 VU meter.
- STEP 10** Remove CNL #1 from the extender card and re-insert into slot #1.

STEP 11 Repeat steps 7 through 13 for channel 2.

6.6.4 Repro/Sync Level Check/Adjustment

Necessary Tools: - MRL Test Tape

Prerequisites:

- Complete Cleaning and Demagnetizing
- Head Wrap and Azimuth Check/Adjustment
- Secondary Gap Compensation Check/Adjustment

Specification: - All channels will read 0VU +/- 0.2VU.

Once it is determined what speed the machine will be operating at (30ips, 15ips or 7.5ips) for the particular session, a check/adjustment procedure is performed to ensure the optimum performance of the tape recorder. First, the machine should be thoroughly cleaned and demagnetized. Second the head wrap and azimuth must be checked. The third step is to ensure proper playback level adjustment. The fourth step is to ensure proper high frequency equalization of the playback circuitry. The fifth and final step is to check/adjust the record level and high frequency equalization.

This section will deal with the Repo and Sync level check/adjustment procedure. The Repo and Sync level check/adjustments are made using the appropriate test tape (30ips, 15ips or 7.5ips). This will ensure that the APR-5000 Repo and Sync circuitry level adjustment is set properly to the reference fluxivity desired.

6.6.4.1 Repro/Sync Level Check Procedure

STEP 1 Turn the APR-5000 power switch ON.

STEP 2 Load the appropriate test tape onto the machine and select the desired speed. Ensure that none of the channels are in RECORD READY mode. Refer to the NOTE at the bottom of page 6-43 for information on easy access to the test tones on MRL alignment tapes.

STEP 3 Locate to the 1kHz tone of the test tape.

STEP 4 Select REPRO mode by pressing the REPRO key on the meter bridge. Playback the 1kHz tone and observe the meter readings. If any of the VU meters display a reading other than 0VU, perform the adjustment procedure in Section 6.6.4.2.

STEP 5 Select SYNC mode by pressing the SYNC key on the meter bridge. Playback the 1kHz tone and observe the meter readings. If any of the VU meters display a reading other than 0VU, perform the adjustment procedure in Section 6.6.4.2.

6.6.4.2 Repro/Sync Level Adjustment Procedure

STEP 1 Select REPRO mode by pressing the TAPE key on the meter bridge.

STEP 2 Locate to the beginning of the 1kHz tone.

STEP 3 Press the IND key (on the ALN Panel) to access the channel needing adjustment, and press PLAY.

STEP 4 Press the LEVEL key in the Repro section of the ALN Panel.

STEP 5 Press the INC or DEC keys in the Calibration section of the ALN Panel to adjust the repro playback level to equal 0VU on the meter.

STEP 6 Repeat STEPs 2 through 5 for any other channels that require adjustment.

STEP 7 Press the SYNC key on the meter bridge. This will (when the machine is in PLAY mode) automatically select SYNC mode.

STEP 8 Repeat STEPs 2 and 3.

STEP 9 Press the LEVEL key in the Sync section of the ALN Panel.

STEP 10 Repeat STEPs 5 and 6 for the Sync circuits.

NOTE: It is important to ensure that only the 1kHz tone is used for this check/adjustment procedure. This will require locating to the beginning of the test tone several times during the course of the procedure. To help reduce the procedure time, utilize the REPEAT function. Store the tape timer reading of the beginning of the desired tone in memory location 28 and the tape timer reading of the end of the tone into memory location 29. After doing this, press the REPEAT key. This will place the APR-5000 into REPEAT mode. This means that the machine will playback the section of tape between the two tape locations stored in memory locations 28 and 29. Remember that the value of memory location 29 **MUST** be greater than the value of memory location 28 for the operation to be accepted by the CPU.

6.6.5 Repro/Sync High Frequency Response Check/Adjustment

Necessary Tools: - MRL Test Tape

Prerequisites:

- Complete Cleaning and Demagnetization
- Head Wrap and Azimuth Check/Adjustment
- Secondary Gap Compensation Check/Adjustment
- Repro/Sync Level Adjustment

Specification: - All meters will read \emptyset VU +/- $\emptyset.2$ VU.

The Repro and Sync high frequency check/adjustment is made utilizing the appropriate test tape for the desired speed that the alignment is required. Ensure that the prerequisite procedures are done prior to performing this procedure. As stated in the specification, the Repro and Sync high frequency playback response should be set to read \emptyset VU +/- $\emptyset.2$ VU.

6.6.5.1 Repro/Sync High Frequency Response Check Procedure

STEP 1 Turn the APR-5000 power switch ON.

STEP 2 Select the desired speed (30ips, 15ips or 7.5ips).

STEP 3 Select REPRO mode by pressing the REPRO key on the meter bridge.

STEP 4 Load the appropriate test tape onto the machine, and locate the 10kHz tone. Refer to the NOTE at the bottom of page 6-45 for assistance on location of the 10kHz tone on the MRL test tapes.

STEP 5 Press the PLAY key, and observe the VU meter readings. All channels should read \emptyset VU +/- $\emptyset.2$ VU. If it is required to adjust any channel, perform the adjustment procedure in Section 6.6.5.2.

STEP 6 Press the SYNC key. This will (when the machine is in PLAY mode) place the machine into SYNC mode and the VU meters will read the Sync head playback signal.

STEP 7 Repeat STEP 5 for SYNC mode.

6.6.5.2 Repto/Sync High Frequency Response Adjustment Procedure

- STEP 1 Press the REPRO key on the meter bridge. This will place the machine into REPRO mode.
- STEP 2 Locate to the beginning of the 10kHz tone.
- STEP 3 Press the IND key to access the channel(s) requiring adjustment.
- STEP 4 Press the H.FREQ key in the Repto section of the ALN Panel.
- STEP 5 Press the PLAY key. This will place the machine into PLAY mode, and signal will be present on the VU meters.
- STEP 6 Press the INC and/or DEC keys in the Calibration section of the ALN Panel to adjust the signal level reading on the bargraph to 0VU +/- 0.2VU.
- STEP 7 Repeat STEP 6 for all channels requiring adjustment. To access the remaining channels, press the IND key until the ALN section of the meter bridge indicates the channel number desired.
- STEP 8 Press the SYNC key. This will (when in PLAY mode) place the machine into SYNC mode which will allow the Sync head playback signal to be displayed on the bargraph meters.
- STEP 9 Repeat STEPs 2 and 3 for SYNC mode.
- STEP 10 Press the H.FREQ key in the Sync section of the ALN Panel.
- STEP 11 Repeat STEPs 5 through 7 for SYNC mode.

6.6.6 Audio System Record Calibration Check/Adjustment

Necessary Tools: - Frequency Generator
- ACVM

Prerequisites: - Complete Cleaning and Demagnetization
- Head Wrap and Azimuth Check/Adjustment
- Repro/Sync Playback Level
Check/Adjustment
- Repro/Sync High Frequency Response
Check/Adjustment
- Secondary Record Compensation
Check/Adjustment

Specification: - As shown in each procedure in this
section.

This section contains the procedures required to check and adjust the record circuitry of the APR-5000. Use these procedures to check and adjust the complete record circuitry alignment. It is necessary to utilize this procedure when; calibrating for a different tape formulation; calibrating for a new headstack; or when an alternative to the alignments stored in memory are desired. It is a good idea to work from an existing alignment that is relatively close to the new alignment in order to save time during the adjustment process.

**** CAUTION ****

The tape used for the record calibration will be the deciding factor of how the alignment is set. Never use old tapes to adjust the record circuitry calibration. This may result in an alignment which is less than optimum for the type of tape being used. Of course for optimum performance the reel of tape that is to be used for the session should be used to calibrate the record circuitry. In some cases this is not possible. If so, use the same tape type (formulation) as the session tape for the alignment of the record circuitry.

Once the heads have been properly aligned for good tape path and proper playback frequency response, the record system must also be aligned so that the recorded signals will be played back with a flat frequency response characteristic.

There is an extremely complex relationship between bandwidth, distortion, tape velocity, and the amplitude of the bias signal recorded on the tape. This relationship varies for tapes of alternate formulations, and of course the same tape aligned in different ways. When aligning the audio, the calibration is made such that the optimum levels of bias frequency, high and low frequency equalization and output

level which provide the greatest high frequency range with the lowest third order harmonic distortion.

The amount of record level and bias level determines the fluxivity level of the signal recorded on the tape. The amount of fluxivity will directly affect the harmonic distortion. The amount of bias is determined by the amount the bias signal is adjusted beyond the peak. For this reason, this adjustment is referred to as "overbias". The point at which the overbias is set will vary from tape to tape, from one formulation to another, with different heads and with different tape speeds. This may cause some confusion when selecting the proper overbias setting. For more information on overbias settings contact the Sony Regional Service Representative.

For general purpose operation, it is recommended to select an overbias setting that both preserves the high frequency response and provides the lowest distortion in the peak program area (a level that the recorded program material does not attain on a regular basis). It may be advantageous in some cases to record the program material at a fluxivity that provides more high frequency loss and a lower distortion content. For this reason the actual overbias setting is at the discretion of the user.

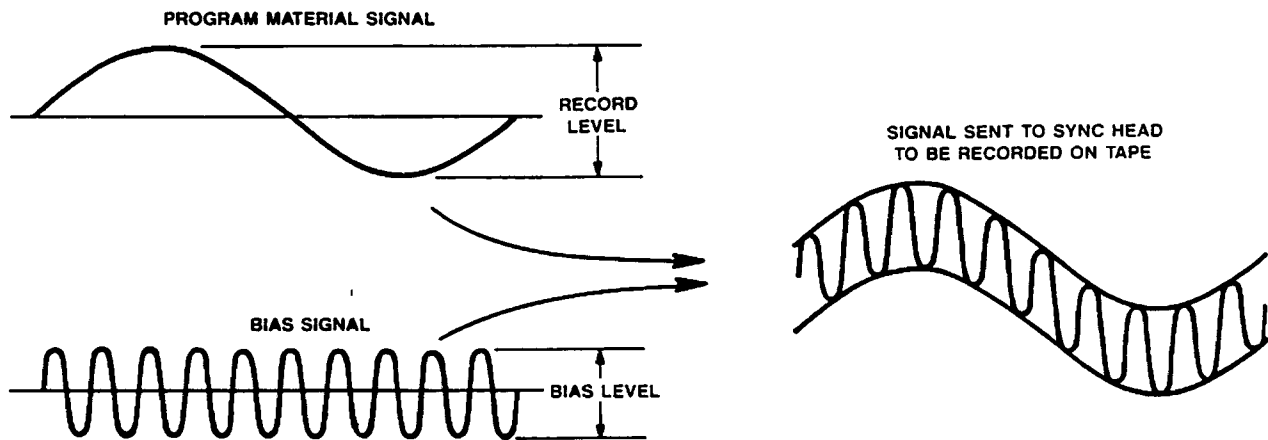


Figure 6-31. Record Level/Bias Level

6.6.6.1 Record Level/Bias Level Check/Adjustment Procedure

The RECORD LEVEL adjustment is made to set the amplitude of the program material signal which is recorded onto the tape. The BIAS LEVEL adjustment is made to set the amplitude of the bias signal (which is intermixed with the program material) so that the program material signal that is recorded onto the tape has the desired balance of high frequency loss and distortion, as discussed in Section 6.6.6. Refer to Figure 6-30. Generally the bias level setting is referred to as overbias because the amplitude of the bias signal is set to cause a loss of a few dB at the high frequency range. These adjustments are interactive and are critical in obtaining optimum audio performance in the recordings produced by the APR-5000.

- STEP 1 Turn the APR-5000 power switch ON.
- STEP 2 Connect the test equipment as shown in Figure 6-22.
- STEP 3 Load the recording tape onto the machine (refer to the CAUTION note in Section 6.6.6). Ensure that the tape has been fully erased.
- STEP 4 Press the IND key on the ALN Panel until the STATUS display reads "1".
- STEP 5 Select HI SPEED and press the LEVEL key in the INPUT section of the ALN Panel.
- STEP 6 Adjust the frequency generator (or console oscillator) to inject a 10kHz sine wave at +4dBm into the machine. This will produce a reading on the (properly adjusted) channel 1 VU meter of 0VU.
- STEP 7 Select RECORD READY mode for all tracks.
- STEP 8 Press the PLAY and RECORD buttons (either on the remote unit or the transport control panel). This will place the machine into record mode.
- STEP 9 Press the LEVEL key in the BIAS section of the ALN Panel. This will place all channels into BIAS LEVEL ADJUST mode.
- STEP 10 Manipulate the INC or DEC key until the VU meter of the channel being adjusted attains a peak reading. At this point there will not be any overbias applied to the signal being recorded onto the tape.
- STEP 11 Continue to increment until the desired amount of overbias is achieved. Typical values for Scotch 226 are: 1.5dB at 30ips, 2.0dB at 15ips and 7.5ips.

- STEP 12** Press the IND key on the ALN Panel so that the STATUS display reads "2".
- STEP 13** Repeat STEPs 9 through 11.
- STEP 14** Press the IND key until the STATUS display reads "1".
- STEP 15** Adjust the frequency generator (or console oscillator) to 1kHz.
- STEP 16** Press the LEVEL key in the RECORD section of the ALN Panel.
- STEP 17** Manipulate the INC or DEC key for a reading of 0VU on the CH-2 VU meter of the meter bridge.
- STEP 18** Press the LEVEL key in the INPUT section of the ALN Panel.
- STEP 19** Manipulate the INC or DEC key for a reading of 0VU on the CH-2 VU meter on the meter bridge.
- STEP 20** Switch between INPUT LEVEL and RECORD LEVEL, and check the readings for each mode. These adjustments are interactive and may require fine adjustment. Manipulate the INC or DEC key in both modes to attain a reading of 0VU.
- STEP 21** Press the IND key on the ALN Panel until the STATUS display reads "2".
- STEP 22** Repeat STEPs 16 through 20.

6.6.6.2 Record High Frequency Check/Adjustment

The record high frequency adjustment is made to set the record circuitry high frequency equalizer. It is done while in the RECORD mode using the tape type for which the alignment is being made. It is very important that the proper tape is used because the adjustment of the record circuitry relies heavily on the tape being used. It is also important to ensure that the secondary record compensations are properly set, the Repro and Sync playback circuitry has been calibrated, and the RECORD LEVEL and BIAS LEVEL adjustments have been made prior to making this alignment. This adjustment MUST be done immediately following the RECORD LEVEL and BIAS LEVEL adjustments. In practice, this adjustment is a continuation of that procedure.

- STEP 1 Adjust the frequency generator (or console oscillator) to inject a 10kHz +4dBm sine wave.
- STEP 2 Press the IND key on the ALN Panel until the STATUS display reads "1".
- STEP 3 Place the tape machine into RECORD mode.
- STEP 4 Press the H.FREQ key in the RECORD section of the ALN Panel.
- STEP 5 Manipulate the INC or DEC key until the reading on the CH-1 VU meter on the meter bridge equals 0VU.
- STEP 6 Press the IND key on the ALN Panel until the STATUS display reads "2".
- STEP 7 Repeat STEPs 4 and 5.

6.6.6.3 Repro Low Frequency Response Check/Adjustment

Due to the fringing effect that occurs when test tapes are played back on a standard tape machine, the Repro low frequency equalizer is adjusted using a low frequency signal that is recorded onto the tape with the Sync head. This is necessary because the test tapes are full track recordings. Refer to Figure 6-32. When the full track recording of the low frequencies from the test tape are played back through a multi-track head, the low frequencies that are recorded in the guard band area are read by the playback head. This will cause a false reading on the meters as more signal is being read by the head than a normally recorded tape would produce.

- STEP 1 Adjust the frequency generator (or console oscillator) to approximately 80Hz (for 30ips) or 40Hz (for 15ips).
- STEP 2 Place the machine into RECORD mode.
- STEP 3 Sweep the frequency generator (or console oscillator) slightly to ensure that a peak reading on the VU meter exists.
- STEP 4 Press the IND key on the ALN Panel until the STATUS display reads "1".
- STEP 5 Press the L.FREQ key in the REPRO section of the ALN Panel.
- STEP 6 Manipulate the INC or DEC key for a +0.5VU reading on the VU meter on the left side of the meter bridge.

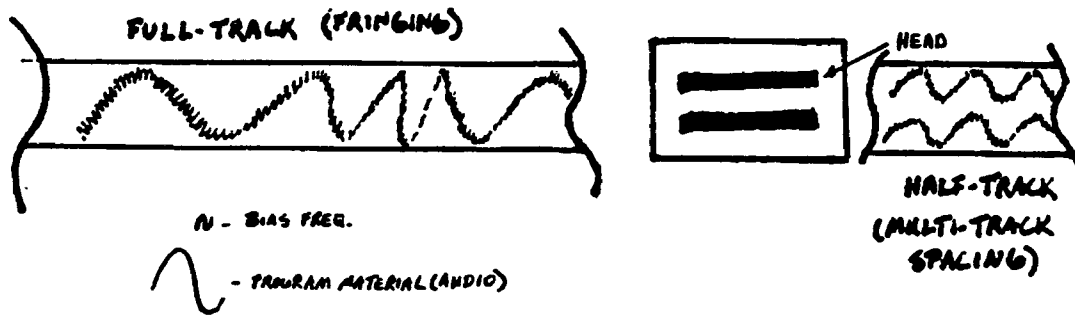


Figure 6-32. Fringing Effect

STEP 7 Press the IND key on the ALN Panel until the STATUS display reads "2".

STEP 8 Repeat STEPs 5 and 6.

6.6.6.4 Sync Low Frequency Check/Adjustment

The reason that the test tape cannot be used for the Repr low frequency alignment (fringing effect) is the same reason that the test tapes cannot be used for the Sync low frequency alignment. Refer to Section 6.6.6.3 for details on fringing effect.

- STEP 1** Set the frequency generator (or console oscillator) to approximately 80Hz (for 30ips) or 40Hz (for 15ips).
- STEP 2** Place the APR-5000 into RECORD mode. Press the REPRO key (for all channels) on the meter bridge. This will place the APR-5000 into REPRO mode for all channels.
- STEP 3** Sweep the frequency generator (or console oscillator) frequency control slightly to ensure that there is a peak.
- STEP 4** Record approximately 4 minutes of this frequency. This recorded tone will be the playback reference for the adjustment of the Sync low frequency equalizer circuit.
- STEP 5** Locate to the beginning of the tone. Place the APR-5000 into PLAY mode.
- STEP 6** Press the IND key on the ALN Panel until the STATUS display reads "1".

STEP 7 Press the **L.FREQ** key in the **SYNC** section of the **ALN** Panel.

STEP 8 Press the **INC** or **DEC** key until the **CH-1 VU** meter on the meter bridge shows a reading of **+0.5VU**.

STEP 9 Press the **IND** key on the **ALN** Panel until the **STATUS** display reads **"2"**.

STEP 10 Repeat **STEPS 7** and **8**.

6.6.7 RCB and RCF Record Compensations

The Record Compensation Feedback (RCB) and the Record Compensation Feedforward (RCF) provide a means to compensate for alternative tape formulations. The standard factory settings are performed using Scotch 226 tape. If it is desired to use another tape type, refer to the chart in Table 6-5 and set the RCB and RCF accordingly. Tapes of less contemporary formulation and possibly those of future formulations may require some deviation from the chart.

****NOTE:** If the battery back-up on the CPU board is lost for any reason, these adjustments will be required for all preset locations.

TAPE TYPE		30 IPS	15 IPS	7.5 IPS
3M Scotch 226	RCF	C0	CB	C4
	RCB	C1	C7	C4
3M Scotch 250	RCF	C0	CB	C4
	RCB	C2	C7	C4
Afga 469	RCF	C0	CB	C4
	RCB	C1	C7	C4
Ampex 456	RCF	C0	CB	C4
	RCB	C1	C7	C4
BASF LGR50	RCF	C0	CB	C4
	RCB	C1	C7	C1
AFGA PER528	RCF	C0	CB	C6
	RCB	C2	C7	C2
BASF LGR30	RCF	C0	CB	C6
	RCB	C2	C7	C2
3M Scotch 176	RCF	C0	C8	C4
	RCB	C2	C7	C4

Table 6-5. RCB and RCF Settings

The RCB provides a control range from C0(hex) to C7(hex). It provides a shelving 2kHz to 8kHz boost with decreasing control codes. Refer to the RCB graph in Figure 6-33. The RCB provides a control range from C0(hex) to CF(hex). It provides a shelving 8kHz to 25kHz high frequency boost with increasing control codes. Refer to the RCF graph in Figure 6-33. To access these adjustments and perform the adjustment procedure, follow the adjustment procedure listed on the below.

- STEP 1** Turn the APR-5000 power switch ON.
- STEP 2** Select HI speed.
- STEP 3** Press the ALL key on the ALN Panel.
- STEP 4** While holding the CONTROL key on the ALN Panel DOWN, press the RCF (LEVEL) key in the RECORD section of the ALN Panel. This will display the setting of the RCF in that speed in the STATUS display. Remember to perform this procedure for both speeds.
- STEP 5** Manipulate the INC or DEC key to adjust the RCF to the desired setting.
- STEP 6** While holding the CONTROL key on the ALN Panel DOWN, press the RCB (H.FREQ) key in the RECORD section of the ALN Panel. This will display the setting of the RCB (in that speed) in the STATUS display. Remember to perform this procedure for both speeds.
- STEP 7** Repeat STEPs 3 through 6 for MID and LO speeds.

6.6.8 RGC and SGC Head Gap Compensation

Head gap compensation for the Repro head (RGC) and the Sync head (SGC) provide a means to compensate for alternate gap-width heads. Refer to Table 6-6 for standard settings.

Repro Gap Compensation (RGC)	30ips.....C 1 15ips.....C A 7.5ips.....C A
Sync Gap Compensation (SGC)	30ips.....C 1 15ips.....C C 7.5ips.....C E

**Table 6-6. RGC and SGC Settings
for High Speed NAB and DIN Heads**

In addition, these adjustments provide for a degree of low frequency response extension for heads of moderate width profile when playing back long wavelength signals. In other words, better low frequency response at 30ips. These control codes provide a shelving high frequency boost from 10 to 25kHz with increasing control codes from C8 (hex) to CF (hex).

Adjusting the gap compensation setting would be required if heads of significantly different gap width are used. Should extensive lapping cause a change in high frequency performance, the gap compensation may be adjusted to compensate.

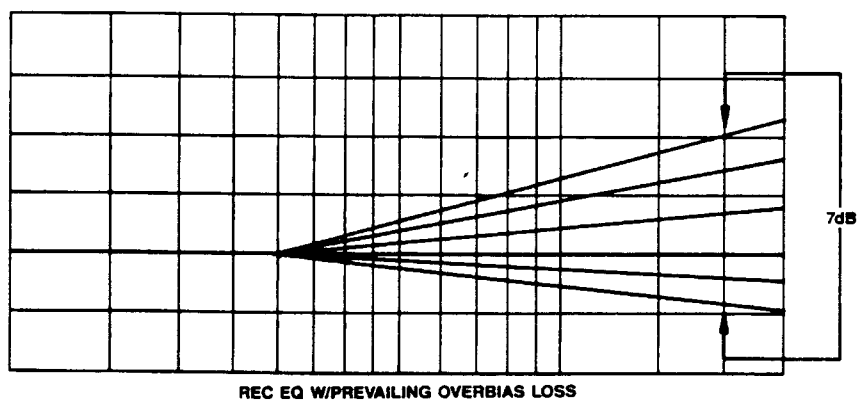
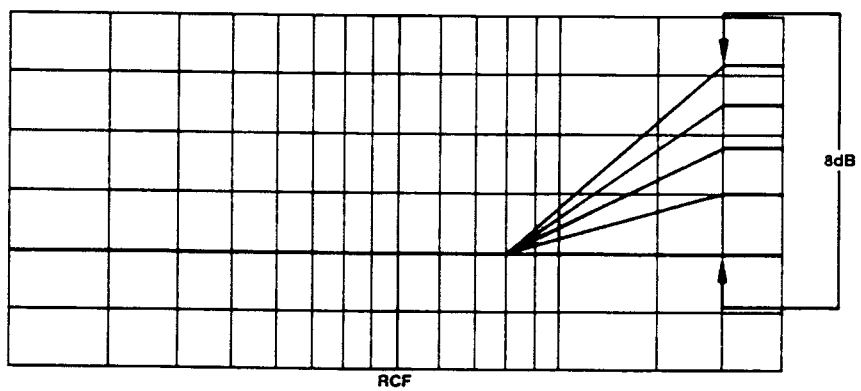
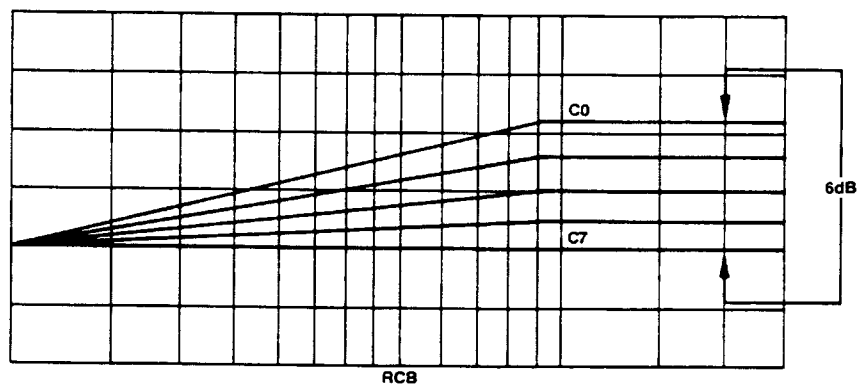


Figure 6-33. Secondary Record Compensations

6.7 Time Code Clock Recovery Check/Adjustment Procedure

Necessary Tools: - Krohn-Hite Function Generator 1000A
- Oscilloscope
- Phillips Head Screwdriver
- Potentiometer Adjustment Tool (tweezer)

The time code clock recovery circuit is located on the CPU board (which is located under the transport control key panel). Adjusting this circuit will optimize the ability of the APR-5000 to interpret both playback time code and external source time code of any variety (SMPTE DF, SMPTE NDF, EBU, or FILM). The time code recovery adjustment ensures correct operation regardless of the time and user bit data within the time code data stream.

STEP 1 Turn the APR-5000 power switch OFF.

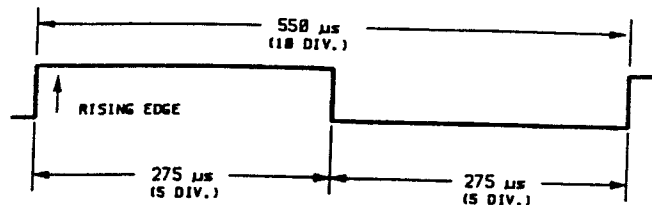
STEP 2 Expose the transport casting by removing the two securing screws on the rear of the top rear cosmetic panel and removing the panel. Remove the two securing screws for the KBD/DSP assembly and opening the transport control key panel.

STEP 3 Remove the three ribbon cables from the CPU board, leaving only the power connector connected.

STEP 4 Turn the APR-5000 power switch ON.

STEP 5 Connect the output of the function generator to CNJ-421 pin 37 of the CPU board, this will be used as the EXT-TC RX signal. This signal should look like the waveform in Figure 6-34.

Monitor on TP3 ... set up scope



*50% Duty Cycle

Figure 6-34. Function Generator Output Waveform (EXT TC RX)

- STEP 6** Connect the positive probe of the oscilloscope to TP9 (EXT RX CLK) on the CPU board.
- STEP 7** Ensure that the waveform that is present at this test point is equivalent to the waveform shown in Figure 6-35 (54% Duty Cycle). If the waveform is not equivalent, adjust RV1 on the CPU board to attain this reading on the oscilloscope.

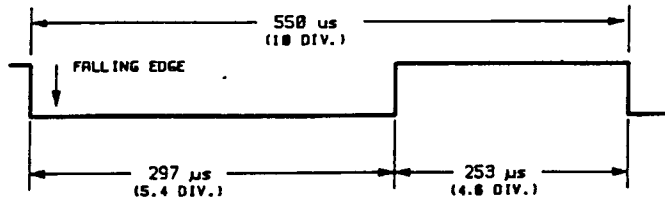


Figure 6-35. EXT RX CLK and PB RX CLK Waveform

- STEP 8** Connect the positive lead of the oscilloscope to TP8 (REC TX CLK) on the CPU board.
- STEP 9** Ensure that the waveform present at TP8 is equivalent to the waveform shown in Figure 6-36. If the waveform is not equivalent, adjust RV3 on the CPU board to attain this reading on the oscilloscope.

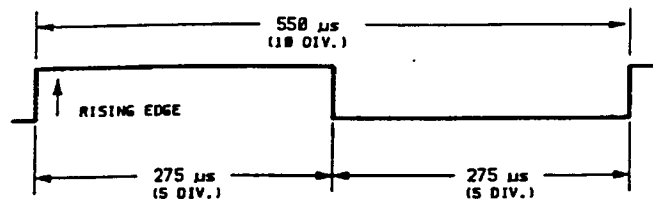


Figure 6-36. REC TX CLK and EXT TC CLK Waveform

- STEP 10** Connect the output of the function generator to TP4 (PB TC RX) of the CPU board.
- STEP 11** Connect the positive lead of the oscilloscope to TP10 (PB RX CLK) of the CPU board.

STEP 12 Ensure that the waveform at TP10 is equivalent to the waveform shown in Figure 6-35. If the waveform is not equivalent, adjust RV2 on the CPU board to obtain this reading on the oscilloscope.

STEP 13 Connect the positive lead of the oscilloscope to TP7 (EXT TX CLK) of the CPU board.

STEP 14 Ensure that the waveform at TP7 (EXT TX CLK) is equivalent to the waveform shown in Figure 6-35. If the waveform is not equivalent, adjust RV4 on the CPU board to obtain this reading on the oscilloscope.

6.8 PC Board Internal Adjustments

The following procedures are not necessary for regular maintenance of the APR-5000. Only in the event of a replacement of the PC board should these adjustments be necessary.

6.8.1 MST Board Bias and Erase Clock Adjustment

Before performing this adjustment, please read Appendix A. The appendix has a complete explanation of Low Frequency Artifact (LFA).

Necessary Tools:

- Oscilloscope
- Extender Card
- Potentiometer Adjustment Tool (tweaker)

Prerequisites: N/A

STEP 1 Remove CNL #1 from card cage.

STEP 2 Inspect D25 on CNL card and note whether it is a glass type or silver epoxy style.

STEP 3 Re-install CNL #1 on an extender card.

STEP 4 Turn APR-5000 ON.

STEP 5 Probe Pin 30B on the extender card and adjust RV1, on the MST card for 9 Vp-p for glass diodes or 12 Vp-p for silver epoxy diodes.

****NOTE:** If you cannot obtain a Frequency Selective Voltmeter:

Adjust RV1, on the MST card for 8.5 Vp-p for glass diodes or 11.5 Vp-p for silver epoxy diodes.

Skip all subsequent STEPs marked with an asterisk "*".

STEP 6 Load a degaussed tape on the unit. Adjust the oscilloscope time/div to 5 msec and volt/div to 50mv. Press RECORD READY for all channels.

STEP 7 Monitoring channel 1 with the oscilloscope (via CAL OUT or LINE OUT), "punch" channel 1 in and out of RECORD and adjust RV4 on the CNL for the minimum LFA.

STEP 8* Set up Frequency Selective Voltmeter as follows:

Resolution Bandwidth	=	3Hz
Frequency Span	=	1kHz
Input Sensitivity	=	+10
Scale	=	90db
Amplitude Ref Level	=	Normal
AFC	=	out

Input a 1kHz +10db sine wave (510nWb/m) on all tracks. Adjust Frequency on voltmeter for maximum level. Press the AFC button. Record tone for 1 minute.

STEP 9* Turn signal generator OFF and rewind tape to the beginning of the tone.

STEP 10* Connect Frequency Selective Voltmeter to CAL OUT or to the line output of channel #1.

STEP 11* Put all channels in RECORD READY and press RECORD.

STEP 12* Ensure depth of erase of -75db or better. Reduce the Master Erase (RV1 on the MST) to the minimum amount needed to achieve Depth of Erase. Check Depth of Erase on Channel 2.

NOTE: Master Erase should NOT be adjusted to a level greater than the minimum required for all tracks to satisfy the Depth of Erase specification.

STEP 13* Re-examine the LFA on channel #1 and adjust CNL Erase symmetry control RV4 for minimum LFA. Typical LFA amplitude is 75mv or less.

STEP 14 Turn APR-5000 OFF.

- STEP 15** Remove CNL #1 from extender card and re-insert it into the unit.
- STEP 16** Remove CNL #2 and re-install it on the extender card.
- STEP 17** Turn APR-5000 ON.
- STEP 18** Press RECORD READY channel #2.
- STEP 19** Alternately pressing record and play, adjust RV4 for minimum LFA.
- STEP 21** Verify depth of erase on all channels of the card cage.

6.8.2 CNL Card BIAS and ERASE Envelope Adjustment

There are adjustments on each of the CNL cards for Bias and Erase ramp symmetry. These adjustments are checked and/or made with the questioned card placed on the extender card and the corresponding channel in RECORD READY mode. The channel is toggled between RECORD and PLAY mode, while checking for the ramp ON and ramp OFF time. The adjustment will set both ramps to the same duration. A symptom of this adjustment being out of specification is, "an unusual punch-in/punch-out noise".

Necessary Tools: - Oscilloscope
- Work Tape (Scotch 226, etc.)
- Potentiometer Adjustment Tool (tweaker)
- Extender Card

Prerequisites: N/A

- STEP 1** Turn the APR-5000 power switch OFF.
- STEP 2** Remove the questioned CNL card, and place it on the extender card. Install the CNL/Extender card assembly.
- STEP 3** Load a work tape onto the machine and place all channels into RECORD READY mode.
- STEP 4** Connect the oscilloscope probe to pin 6A of the extender card.
- STEP 5** Set the oscilloscope to 1V/div and 20msec/div.

- STEP 6** Alternately punch-in and punch-out of RECORD mode while observing the waveform on the oscilloscope. Ensure that the ERASE ramp is symmetrical (the ramp-on time equals the ramp-off time). If adjustment is necessary, use RV4 (on the CNL card) to adjust the symmetry.
- STEP 7** Connect the oscilloscope probe to pin 5A of the extender card.
- STEP 8** Repeat STEP 6 (for the BIAS ramp). If adjustment is necessary, use RV5 (on the CNL card).

6.8.3 CNL Offset Voltage Adjustment

When installing a new CNL card or when there is excessive monitor switching transients, the offset voltage potentiometer (RV1) may require adjustment. This transient is due to a DC offset present on the playback signal circuit. The transient is heard when the output amplifiers of the APR-5000 are switched between the playback circuit feed and other signal source lines (i.e. INPUT, DIM). Refer to the procedure below when making this adjustment.

Necessary Tools: - ACVM (Hewlett-Packard 400FL or equivalent)
- Potentiometer Adjustment Tool (tweezer)
- Extender Card

- STEP 1** Turn the APR-5000 power switch to the OFF position.
- STEP 2** Remove the suspected CNL card from the card cage and place the extender card into this slot. Install the suspected CNL card onto the extender.
- STEP 3** Turn the APR-5000 power switch to the ON position.
- STEP 4** Connect the ACVM to the LINE OUTPUT (rear panel) of the suspected channel.
- STEP 5** Enter the DIM and UNDIM modes alternately by pressing the SHIELD DEFEAT key. Adjust RV1 on the CNL card for minimum meter deflection on the ACVM. This adjustment will null the DC offset between the playback circuit feed (to the CNL output amplifiers) and the other signal sources (DIM/UNDIM, LINE INPUT, etc.).

NOTE : It is not necessary to remove the heatsink plate for this adjustment. There is a hole provided for easy access to this adjustment potentiometer.

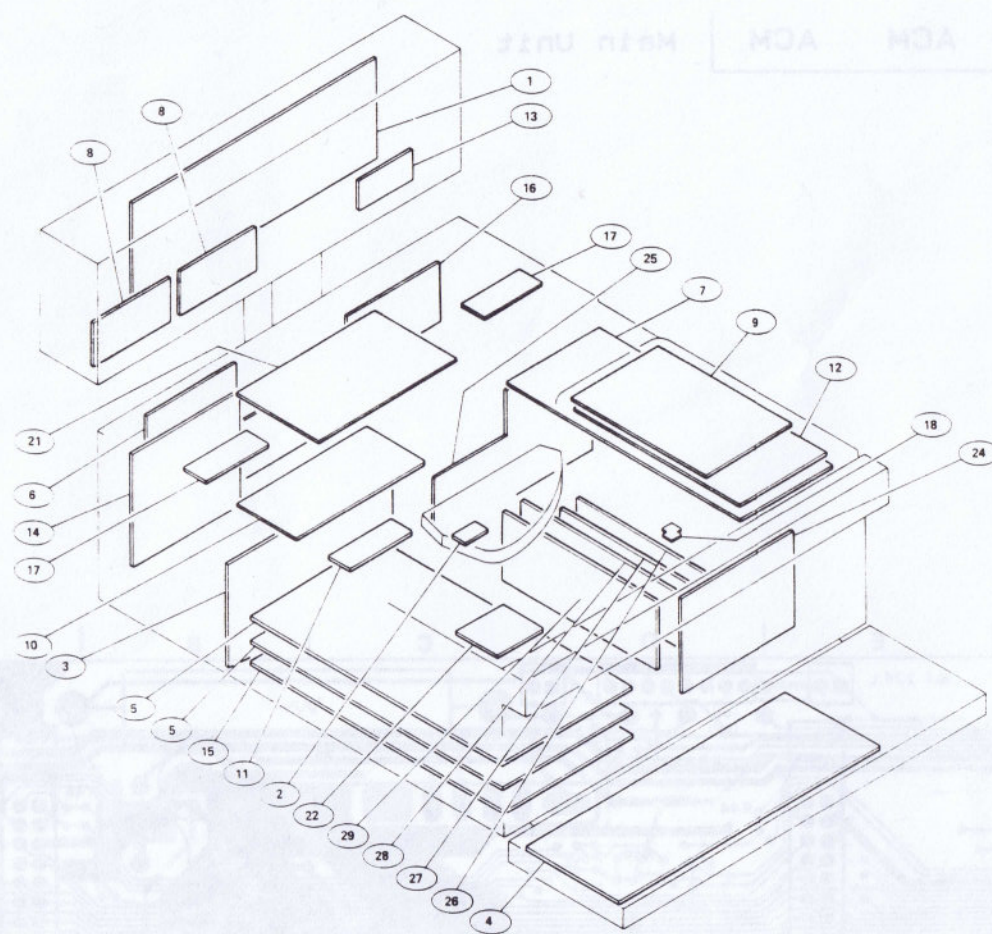
**SECTION 7
SCHEMATIC DIAGRAMS
AND
TECHNICAL DATA**

7.0 Overview

This section contains all schematic diagrams and IC technical Data for the APR-5000 Series machines. Circuit descriptions text for each of the boards are provided in Sections 4 & 5 of this manual. The appropriate text reference pages are listed at the bottom of each schematic diagram.



S/N: APR-5002 20001 TO 20700

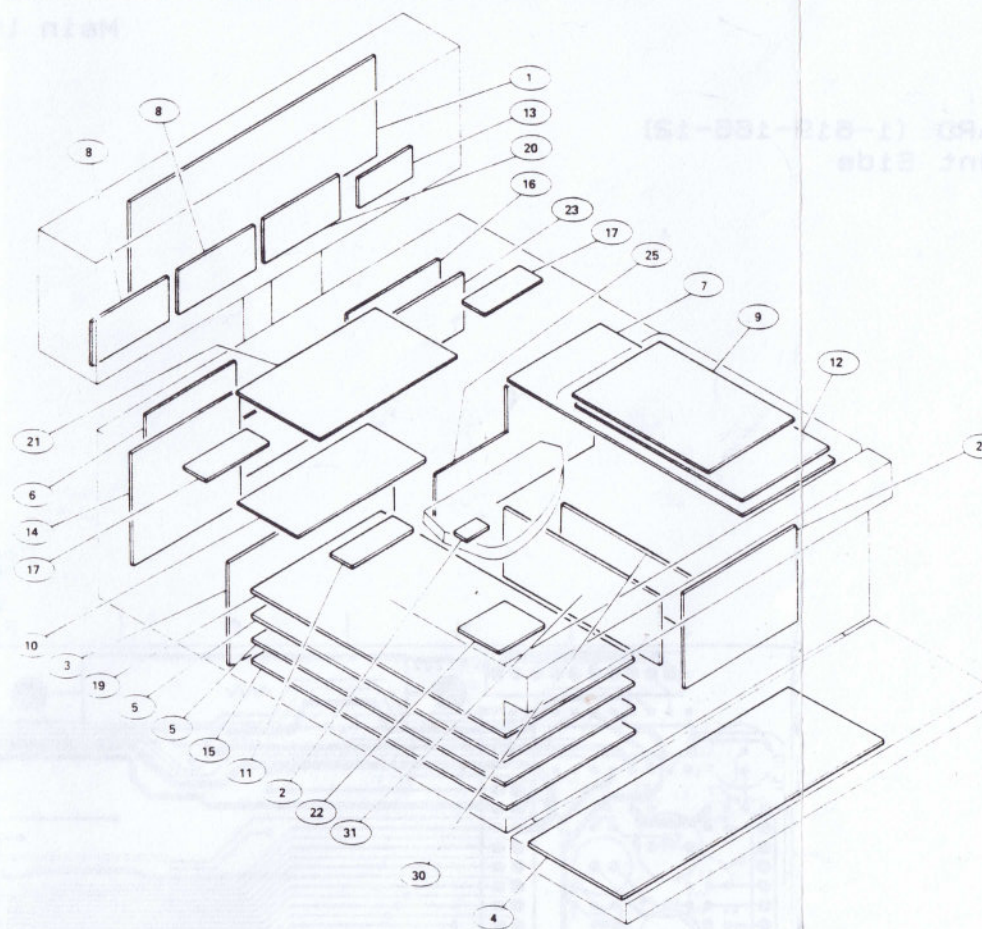


MAIN UNIT

- ① ACM board
- ② AHB board
- ③ ADM board
- ④ ALN board
- ⑤ CNL board
- ⑥ CNX board
- ⑦ CPU board
- ⑧ CTM board
- ⑨ DSP board
- ⑩ FEX board
- ⑪ HES board

- ⑫ KBD board
- ⑬ MSB board
- ⑭ LNT board
- ⑮ MST board
- ⑯ RMD board
- ⑰ RTS board
- ⑱ SBR board
- ⑲ TCC board (For APR-5003V)
- ⑳ TCM board (For APR-5003V)
- ㉑ TIB board
- ㉒ TTS board
- ㉓ VVT board (For APR-5003V)

S/N: APR-5002 20701 AND HIGHER
S/N: APR-5003V 10001 AND HIGHER



POWER SUPPLY

- ⑳ CSL board
- ㉑ PDB board
- ㉒ RGA board
- ㉓ RGB board
- ㉔ RGC board
- ㉕ RGD board
- ㉖ RG-1 board
- ㉗ RG-2 board

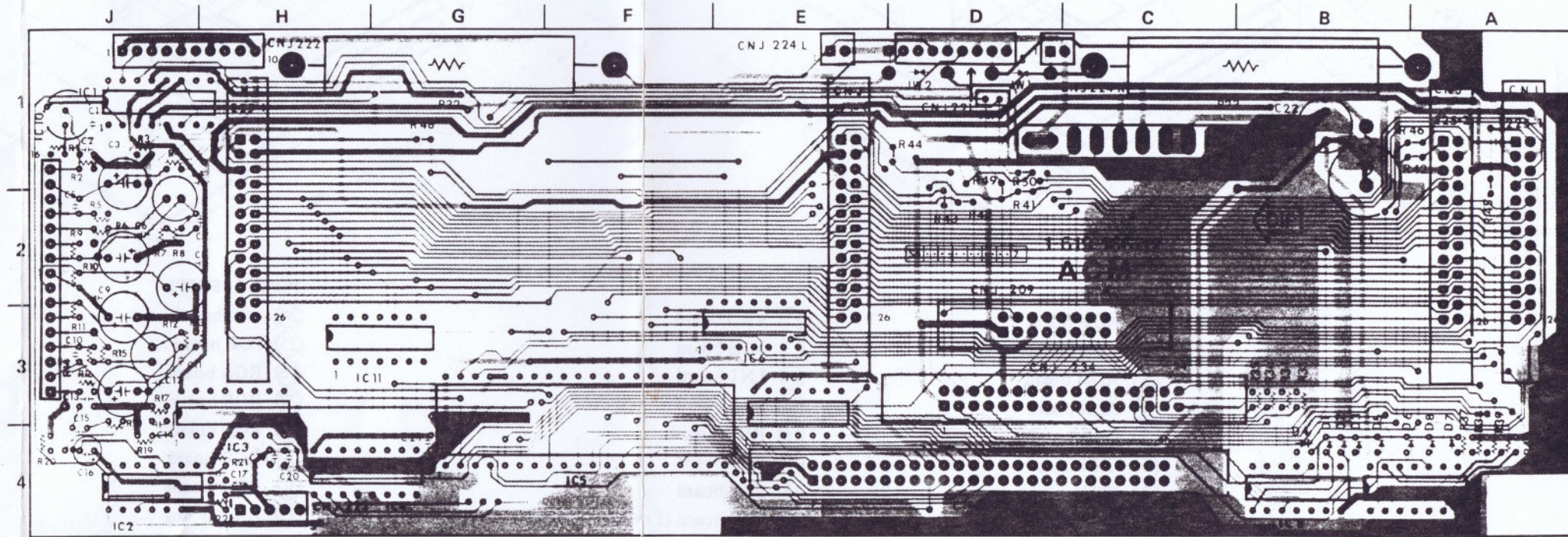
Figure 7-1. PC Board Locations

S/N: APR-5003 10001 AND HIGHER
S/N: APR-5002 50701 AND HIGHER

S/N: APR-5003 10001 TO 20700
S/N: APR-5002 50701 TO 20700

Main Unit | ACM | ACM | Main Unit

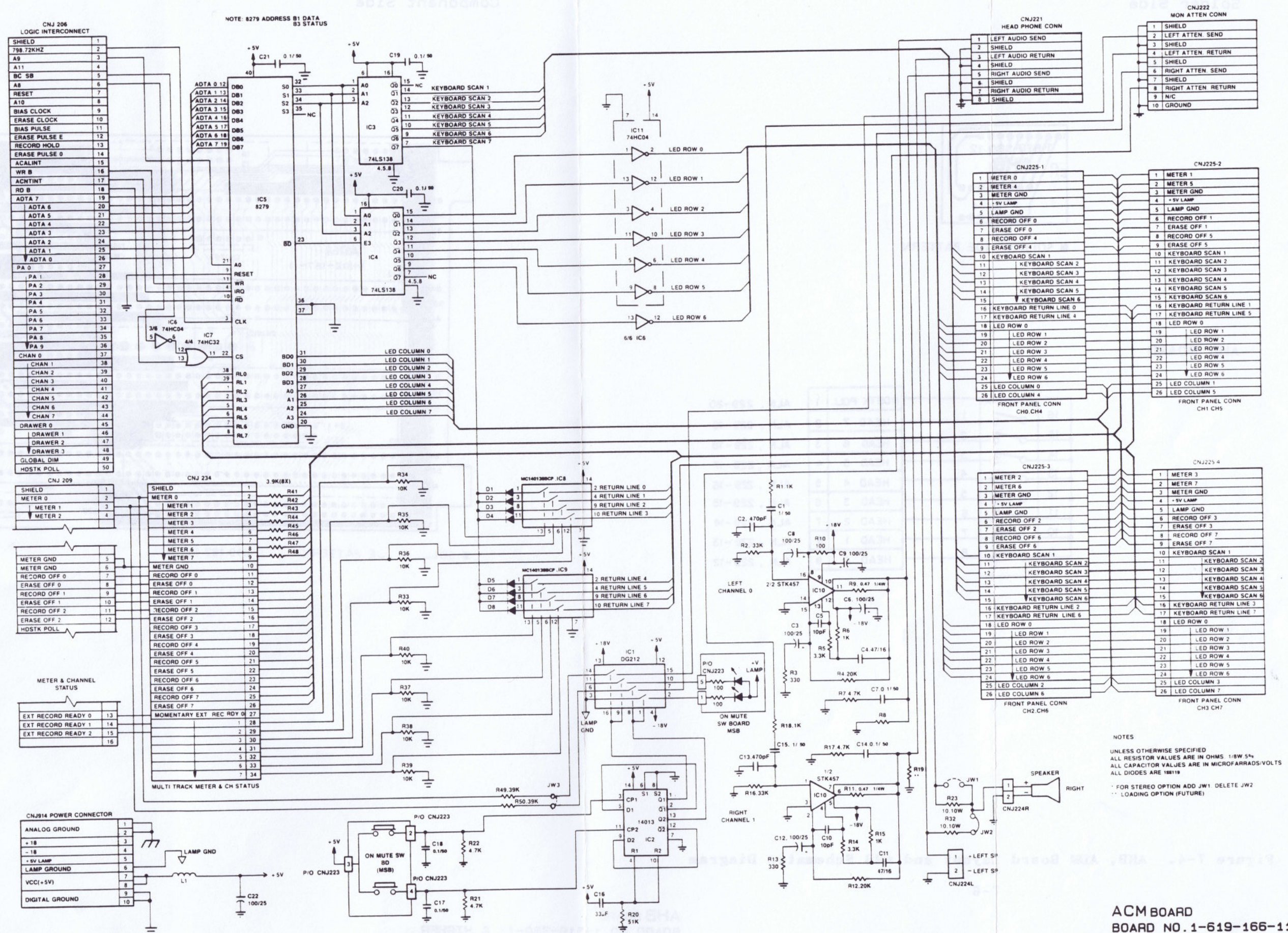
ACM BOARD (1-619-166-12)
Component Side



■ SOLDER SIDE PATTERN 1-619-166-12

Figure 7-2. ACM Board Layout

ACM BOARD



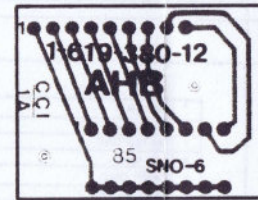
NOTES
 UNLESS OTHERWISE SPECIFIED
 ALL RESISTOR VALUES ARE IN OHMS 1/8W 5%
 ALL CAPACITOR VALUES ARE IN MICROFARRADS/VOLTS
 ALL DIODES ARE 1N9119
 * FOR STEREO OPTION ADD JW1 DELETE JW2
 ** LOADING OPTION (FUTURE)

Figure 7-3. ACM Board Schematic Diagram

ACM BOARD
 BOARD NO. 1-619-166-11 & HIGHER
 APR-5002/5003V

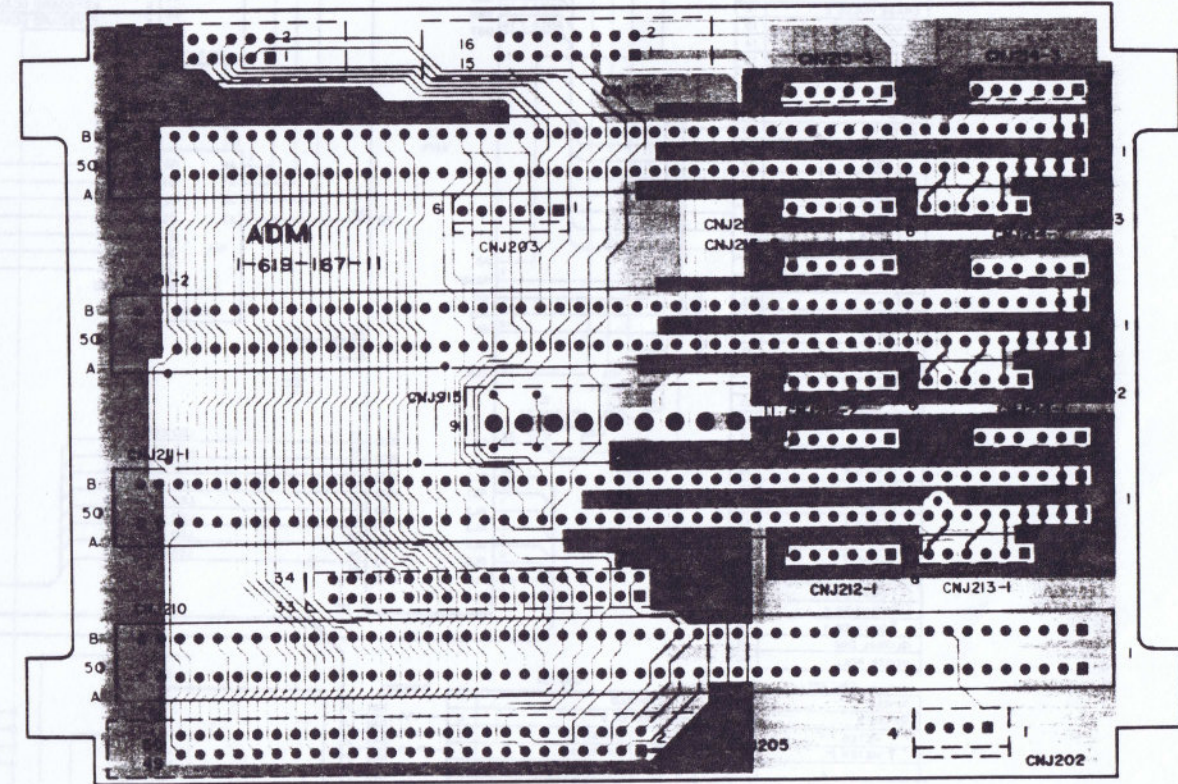
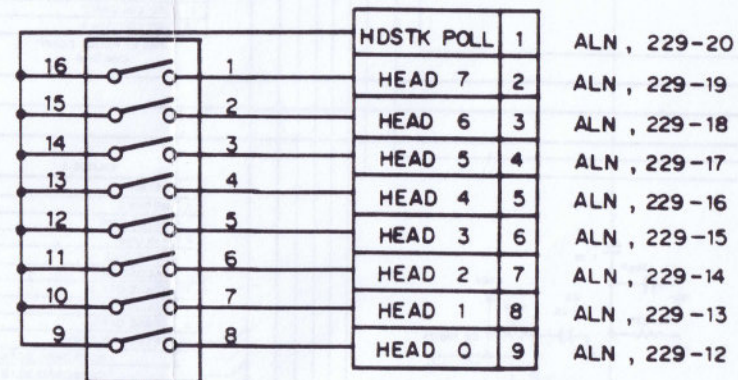
AHB BOARD (1-619-380-12)
Solder Side

ADM BOARD (1-619-167-11)
Component Side



■ SOLDER SIDE PATTERN

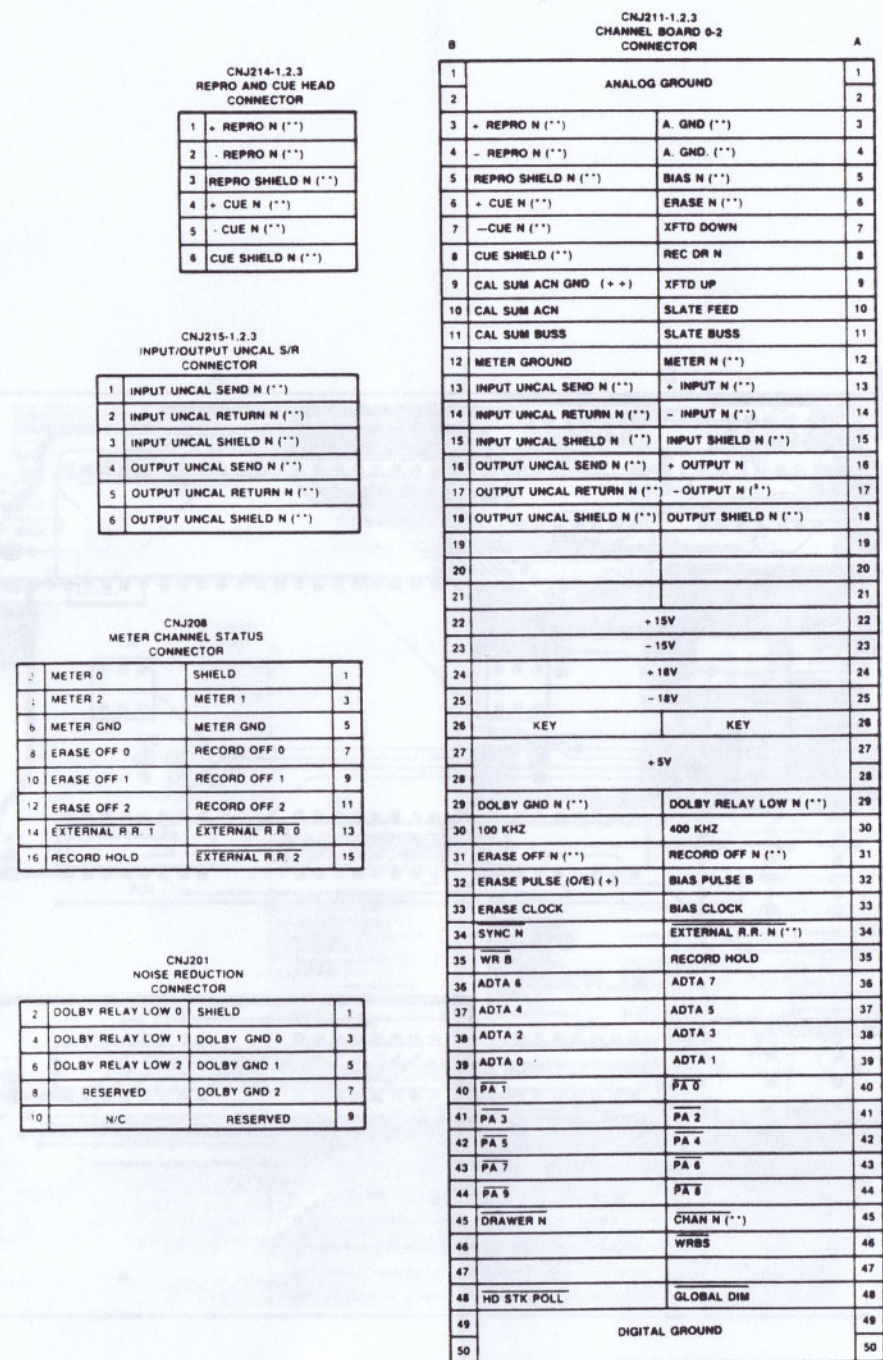
AHB BOARD



■ SOLDER SIDE PATTERN 1-619-167-11

Figure 7-4. AHB, ADM Board Layout and AHB Schematic Diagram

ADM BOARD



CNJ214-1.2.3
REPRO AND CUE HEAD
CONNECTOR

1	+ REPRO N (")
2	- REPRO N (")
3	REPRO SHIELD N (")
4	+ CUE N (")
5	- CUE N (")
6	CUE SHIELD N (")

CNJ215-1.2.3
INPUT/OUTPUT UNCAL S/R
CONNECTOR

1	INPUT UNCAL SEND N (")
2	INPUT UNCAL RETURN N (")
3	INPUT UNCAL SHIELD N (")
4	OUTPUT UNCAL SEND N (")
5	OUTPUT UNCAL RETURN N (")
6	OUTPUT UNCAL SHIELD N (")

CNJ208
METER CHANNEL STATUS
CONNECTOR

2	METER 0	SHIELD	1
1	METER 2	METER 1	3
6	METER GND	METER GND	5
8	ERASE OFF 0	RECORD OFF 0	7
10	ERASE OFF 1	RECORD OFF 1	9
12	ERASE OFF 2	RECORD OFF 2	11
14	EXTERNAL R.R. 1	EXTERNAL R.R. 0	13
16	RECORD HOLD	EXTERNAL R.R. 2	15

CNJ201
NOISE REDUCTION
CONNECTOR

2	DOLBY RELAY LOW 0	SHIELD	1
4	DOLBY RELAY LOW 1	DOLBY GND 0	3
6	DOLBY RELAY LOW 2	DOLBY GND 1	5
8	RESERVED	DOLBY GND 2	7
10	N/C	RESERVED	9

CNJ213-1.2.3
RECORD AND ERASE HEAD

1	BIAS SHIELD (")
2	BIAS N (")
3	ERASE SHIELD (")
4	ERASE N (")
5	SHIELD N
6	REC DR N

CNJ212-1.2.3
INPUT/OUTPUT
CONNECTOR

1	+ INPUT N (")
2	- INPUT N (")
3	INPUT SHIELD (")
4	+ OUTPUT N (")
5	- OUTPUT N (")
6	OUTPUT SHIELD (")

CNJ215
POWER SUPPLY
CONNECTOR

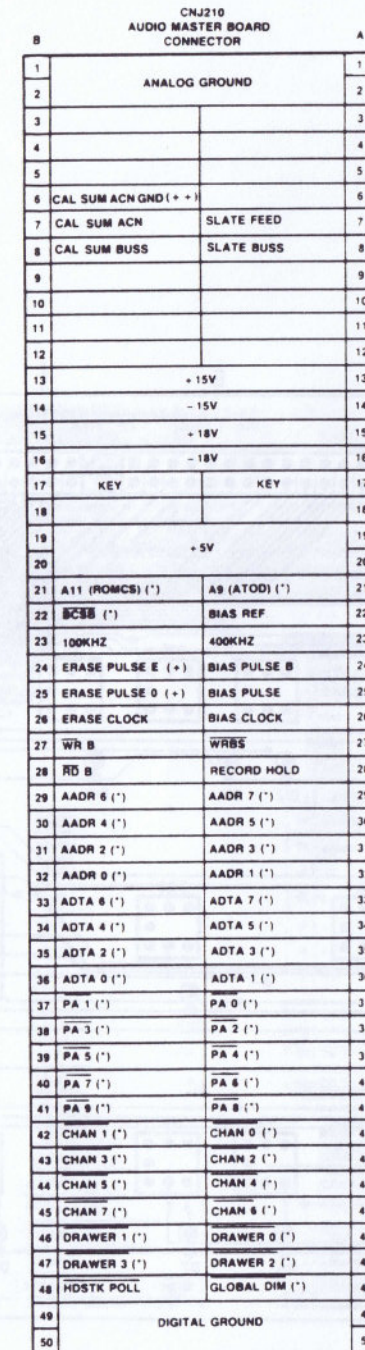
1	
2	ANALOG GROUND
3	+ 18V
4	- 18V
5	+ 5V
6	
7	DIGITAL GROUND
8	
9	KEY

CNJ203
SYNC CONTROL
CONNECTOR

1	+ 5V
2	RESERVED
3	CH2 SYNC
4	CH1 SYNC
5	CHO SYNC
6	A. GND

CNJ200
PROCESSOR INTERFACE
CONNECTOR

2	BCSB (")	SHIELD	1
4	RESET (")	BIAS REF.	3
6	WRBS	BIAS PULSE	5
8	WR B	ACALINT	7
10	RD B	ACNTINT	9
12	AADR 6	AADR 7	11
14	AADR 4	AADR 5	13
16	AADR 2	AADR 3	15
18	AADR 0	AADR 1	17
20	ADTA 6	ADTA 7	19
22	ADTA 4	ADTA 5	21
24	ADTA 2	ADTA 3	23
26	ADTA 0	ADTA 1	25
28	A9	A8 (")	27
30	A11	A10 (")	29
32			31
34			33



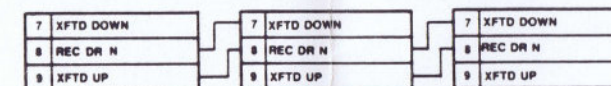
CNJ202
ALIGNMENT I/O
CONNECTOR

1	CAL SUM BUSS
2	SHIELD
3	SLATE FEED
4	SHIELD

CNJ205
LOGIC INTERCONNECT
CONNECTOR

2	BIAS REF	SHIELD	1
4	A11	A9	3
6	A8	BCSB	5
8	A10	RESET	7
10	ERASE CLOCK	BIAS CLOCK	9
12	ERASE PULSE E	BIAS PULSE B	11
14	ERASE PULSE 0	RECORD HOLD	13
16	WR B	ACNLINT	15
18	RD B	ACNTINT	17
20	ADTA 6	ADTA 7	19
22	ADTA 4	ADTA 5	21
24	ADTA 2	ADTA 3	23
26	ADTA 0	ADTA 1	25
28	PA 1	PA 0	27
30	PA 3	PA 2	29
32	PA 5	PA 4	31
34	PA 7	PA 6	33
36	PA 9	PA 8	35
38	CHAN 1	CHAN 0	37
40	CHAN 3	CHAN 2	39
42	CHAN 5	CHAN 4	41
44	CHAN 7	CHAN 6	43
46	DRAWER 1	DRAWER 0	45
48	DRAWER 3	DRAWER 2	47
50	HDSTK POLL	GLOBAL DIM	49

NOTES
 (") REQUIRES PULL UP RESISTOR 10K SIP FROM + 5 VOLTS
 (")N - CHANNEL NUMBER A-0, B-1, C-2
 CHANNEL 0 TO PIN 45A OF CNJ211-1
 EXAMPLE: CHANNEL 1 TO PIN 45A OF CNJ211-2
 CHANNEL 2 TO PIN 45A OF CNJ211-3

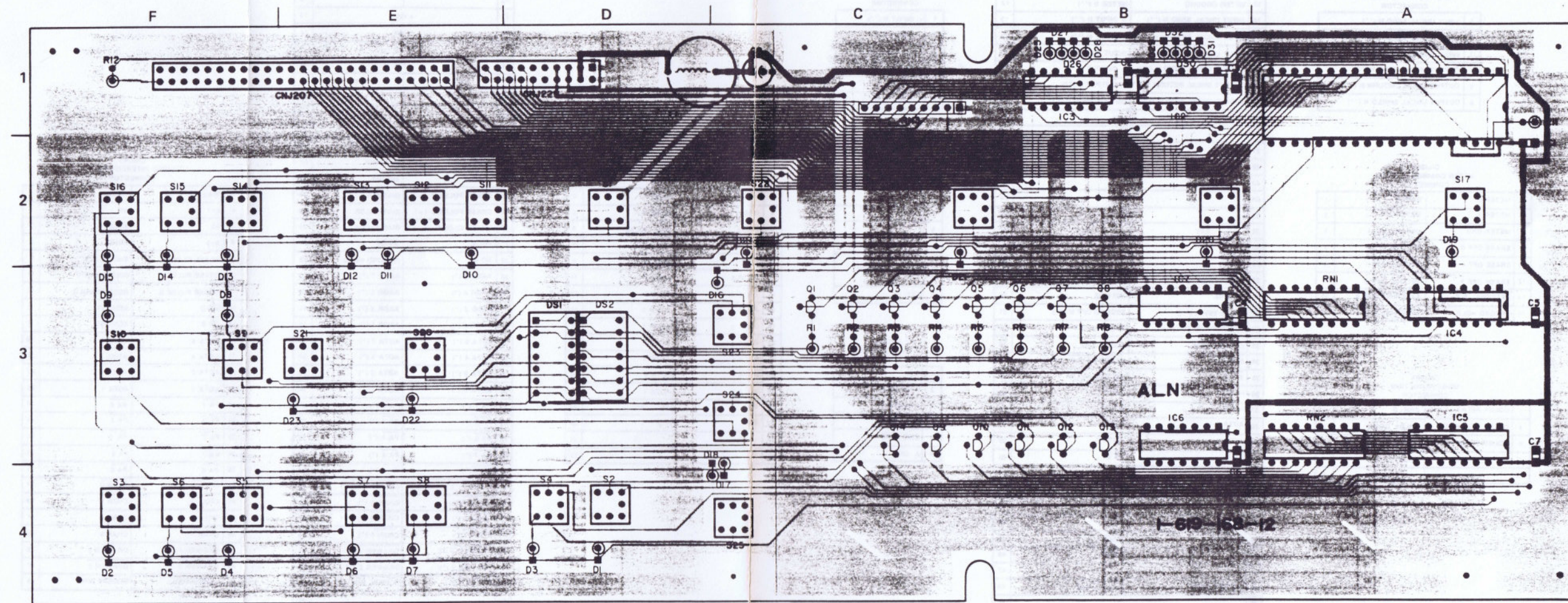


(+) ERASE E TO CNJ211-2 PIN 32B, ERASE 0 TO CNJ211-1.3 PIN 32B
 (++) ALL CAL SUM ACN GNDs ARE BUSSed TOGETHER, NOT TO GROUND

Figur 7-5. ADM Schematic Diagram

XFTD CHART

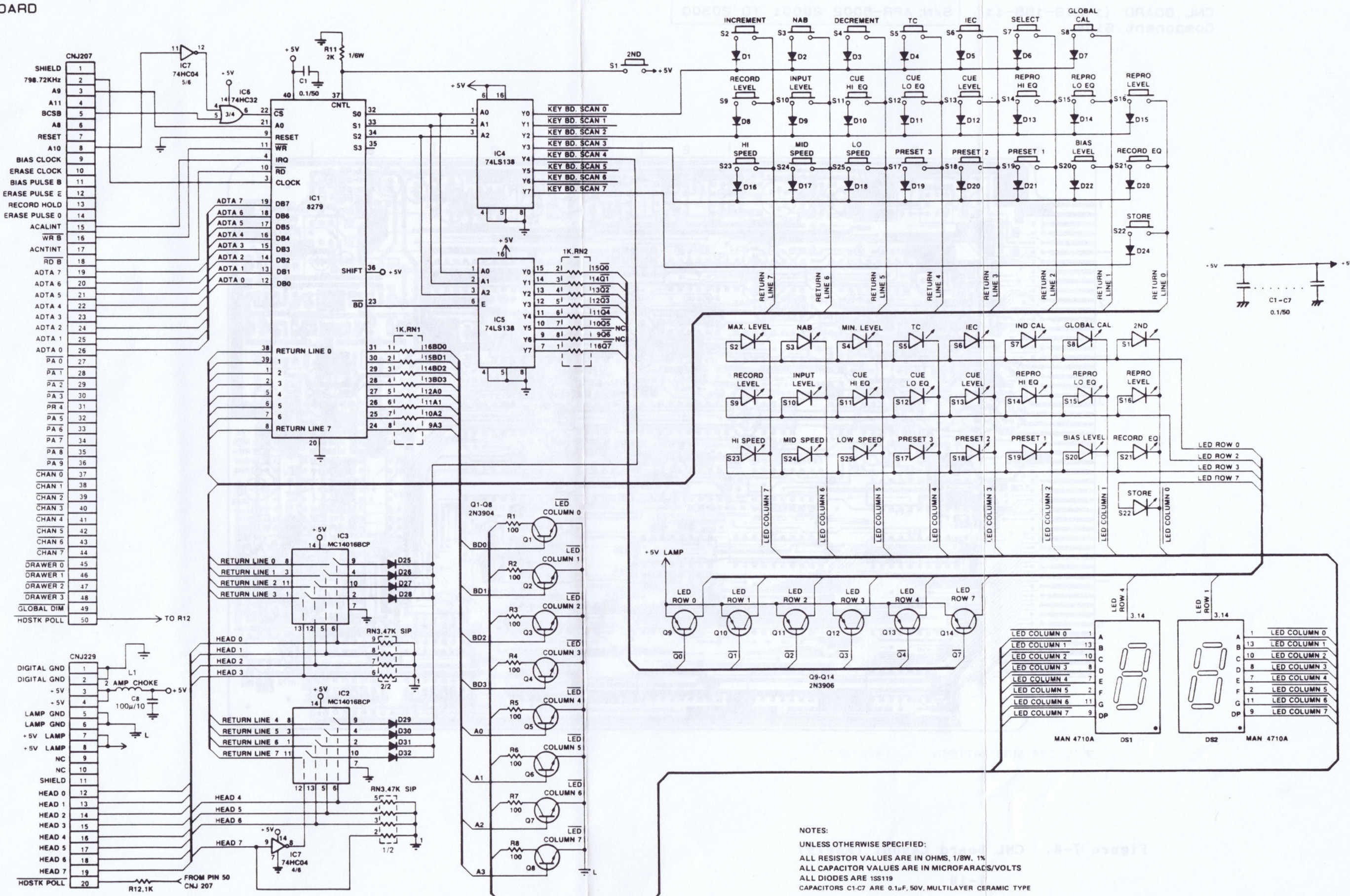
ALN BOARD (1-619-168-12)
Component Side



■ SOLDER SIDE PATTERN 1-619-168-12

Figure 7-6. ALN Board Layout

ALN BOARD



NOTES:
 UNLESS OTHERWISE SPECIFIED:
 ALL RESISTOR VALUES ARE IN OHMS, 1/8W, 1%
 ALL CAPACITOR VALUES ARE IN MICROFARADS/VOLTS
 ALL DIODES ARE 1S119
 CAPACITORS C1-C7 ARE 0.1µF, 50V, MULTILAYER CERAMIC TYPE

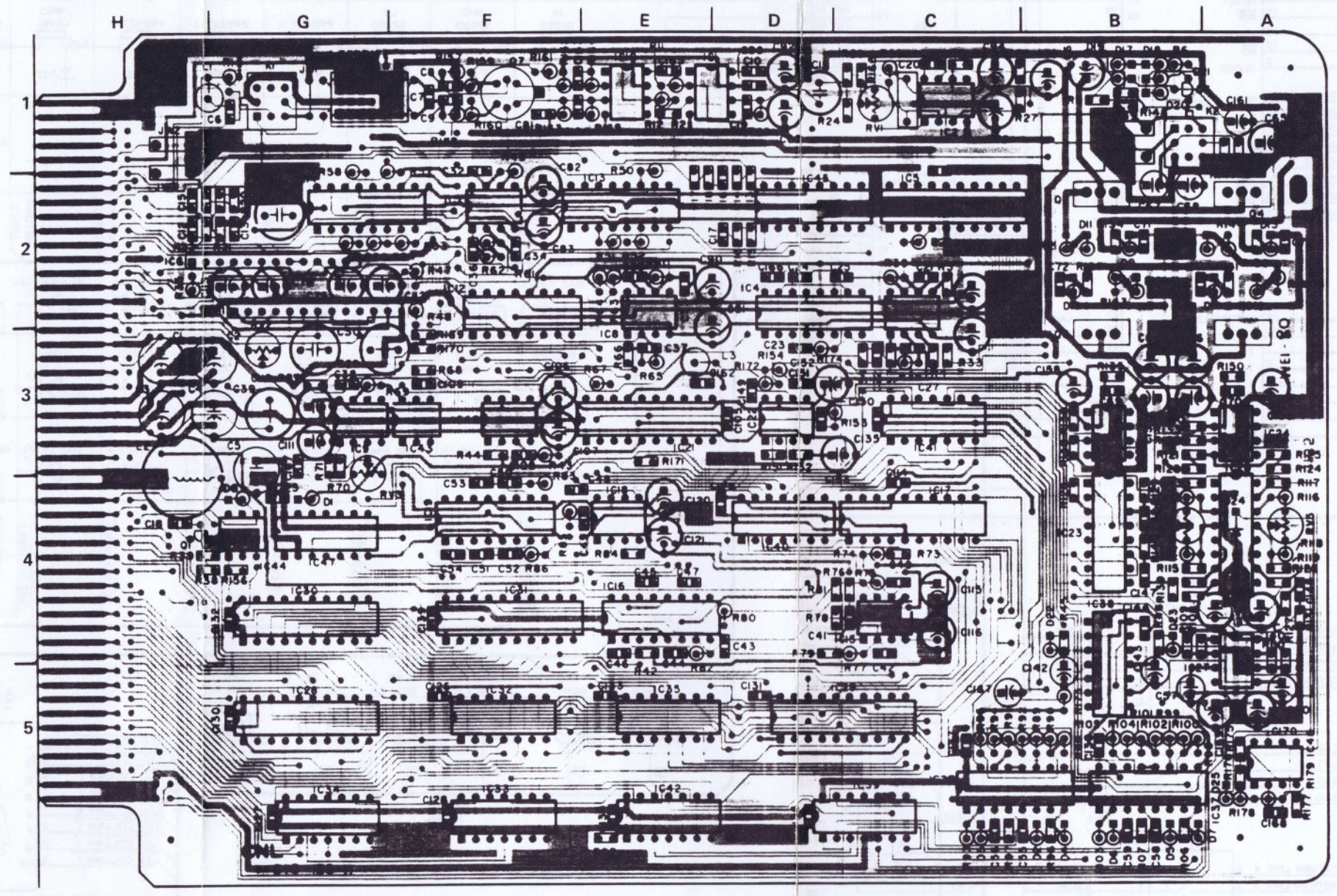
Figure 7-7. ALN Board Schematic Diagram

ALN BOARD
 BOARD NO. 1-619-168-11 & HIGHER
 APR-5002/5003V

CNL BOARD (1-619-158-11)
Component Side

S/N: APR-5002 20001 TO 20300

GRADE KJA



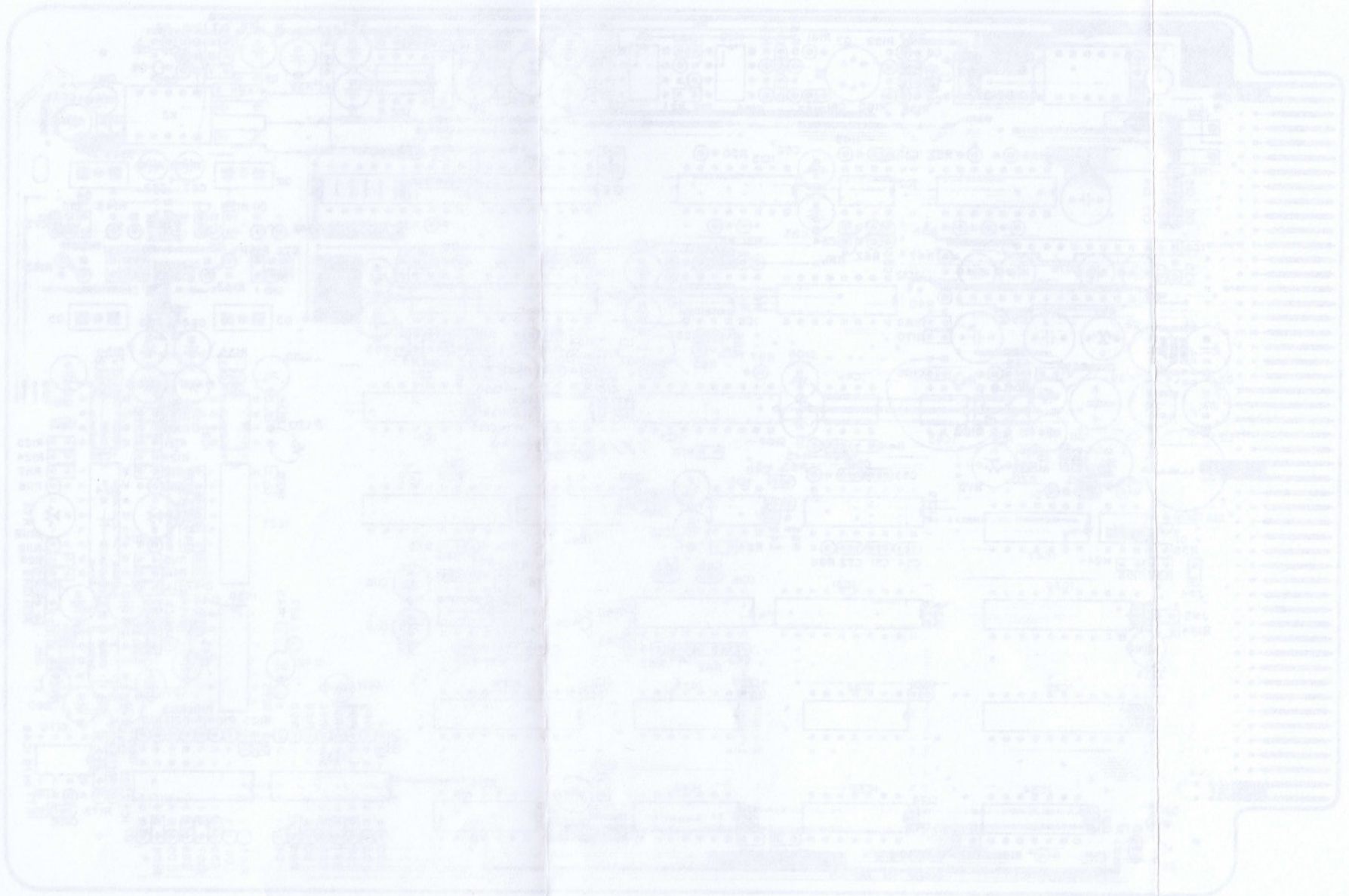
3 SOLDER SIDE PATTERN 1-619-158-11

Figure 7-8. CNL Board Layout (Early)

1	IC1	IC2	IC3	IC4	IC5	IC6	IC7	IC8	IC9	IC10	IC11	IC12	IC13	IC14	IC15	IC16	IC17	IC18	IC19	IC20	IC21	IC22	IC23	IC24	IC25	IC26	IC27	IC28	IC29	IC30
2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	R17	R18	R19	R20	R21	R22	R23	R24	R25	R26	R27	R28	R29	R30
3	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15	C16	C17	C18	C19	C20	C21	C22	C23	C24	C25	C26	C27	C28	C29	C30
4	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30
5	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12	L13	L14	L15	L16	L17	L18	L19	L20	L21	L22	L23	L24	L25	L26	L27	L28	L29	L30

ALM BOARD
BOARD NO. 1-619-158-11
PR-5002/2030

Figure 7-8. CNL Board Component Side Diagram



8 SOLDER SIDE PATTERN 1-612-158-12

Figure 7-3. CRJ Board Layout (this model)

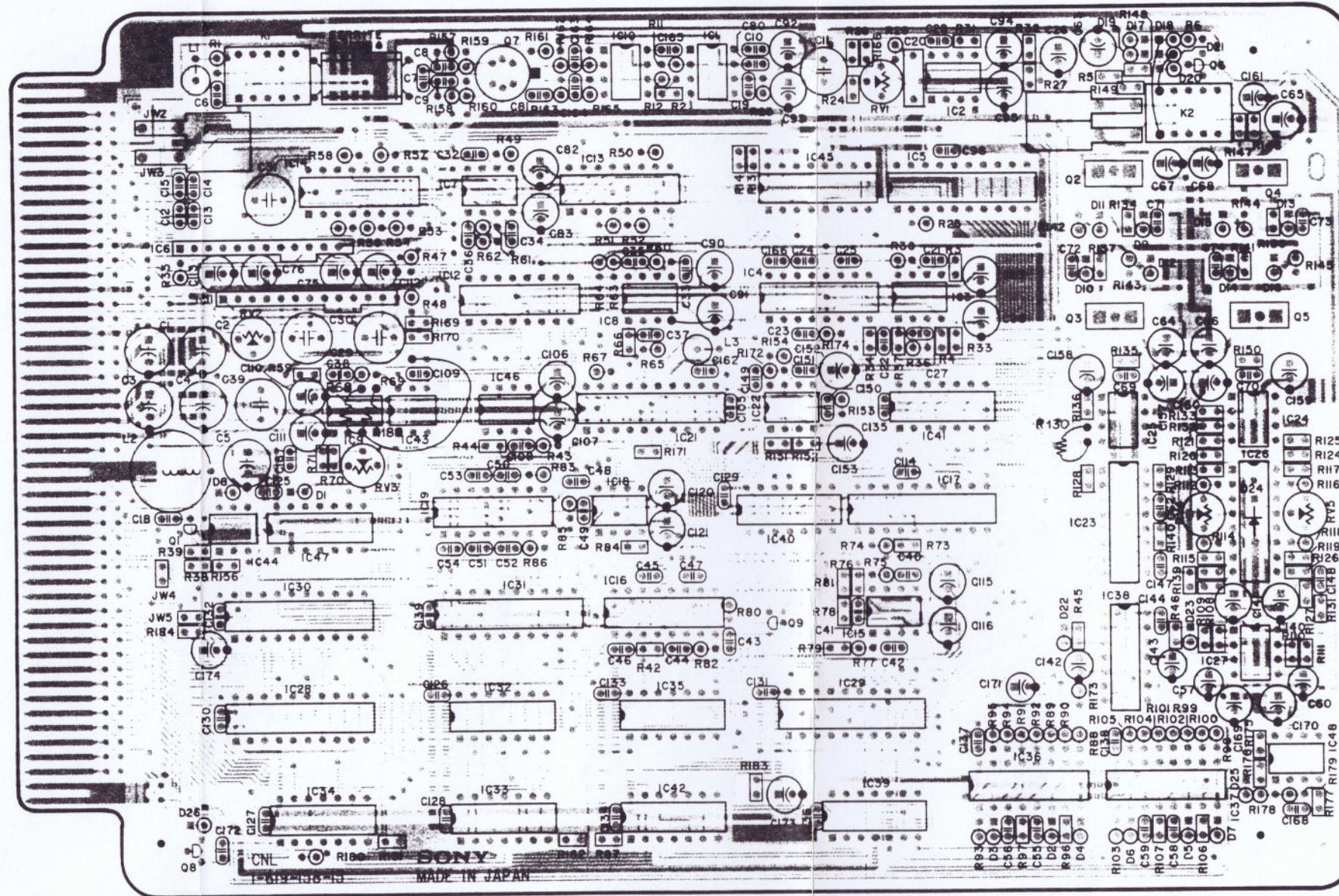
2VN APR-5003V 10001 AND HIGHER
 2VN APR-5002 20301 AND HIGHER

CRJ BOARD (1-612-158-12)
 Component Side

Main Unit CRJ Main Unit

CNL BOARD (1-619-158-15)
Component Side

S/N; APR-5002 20301 AND HIGHER
S/N; APR-5003V 10001 AND HIGHER



■ SOLDER SIDE PATTERN 1-619-158-15

Figure 7-9. CNL Board Layout (Late model)

CNL BOARD

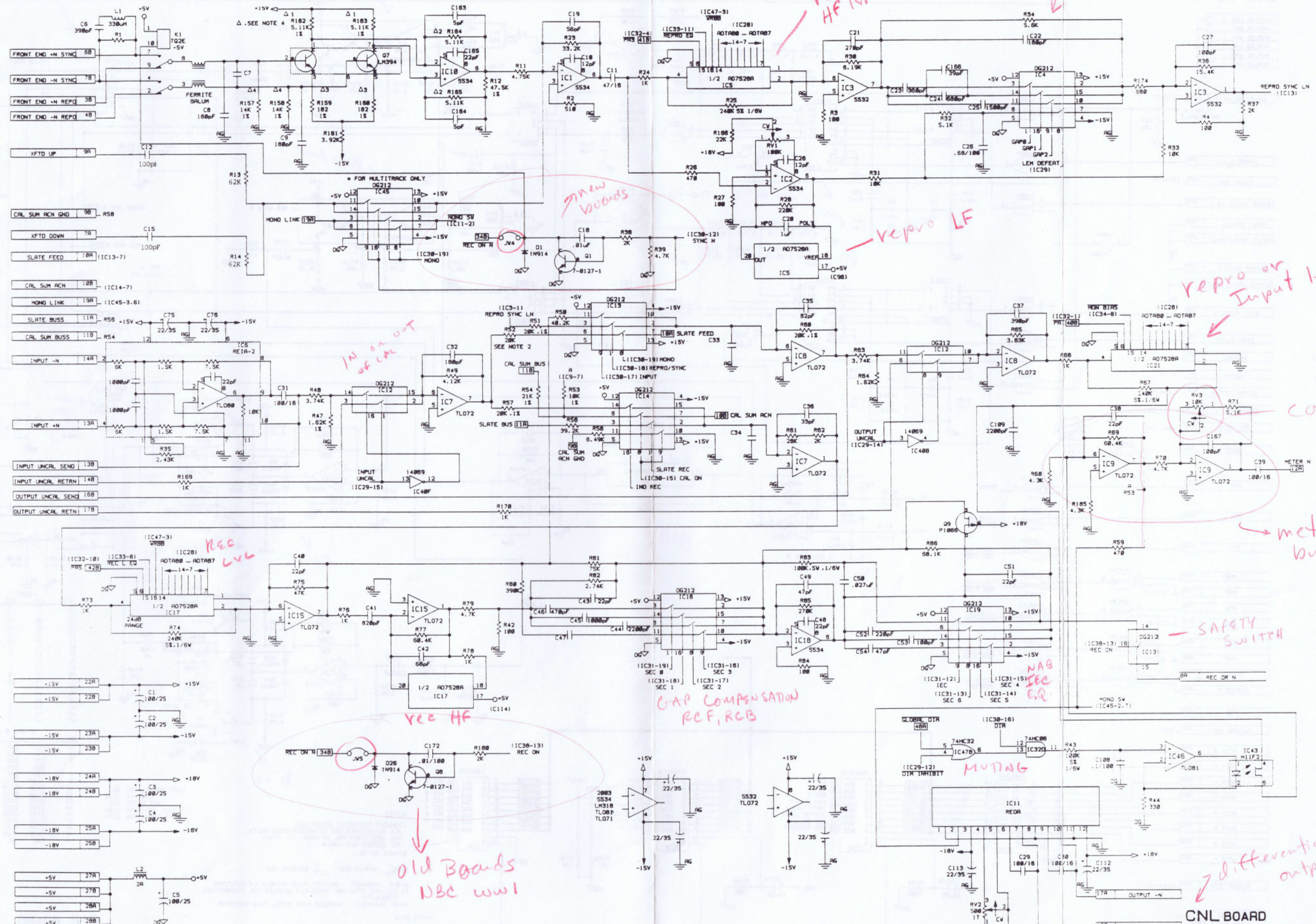
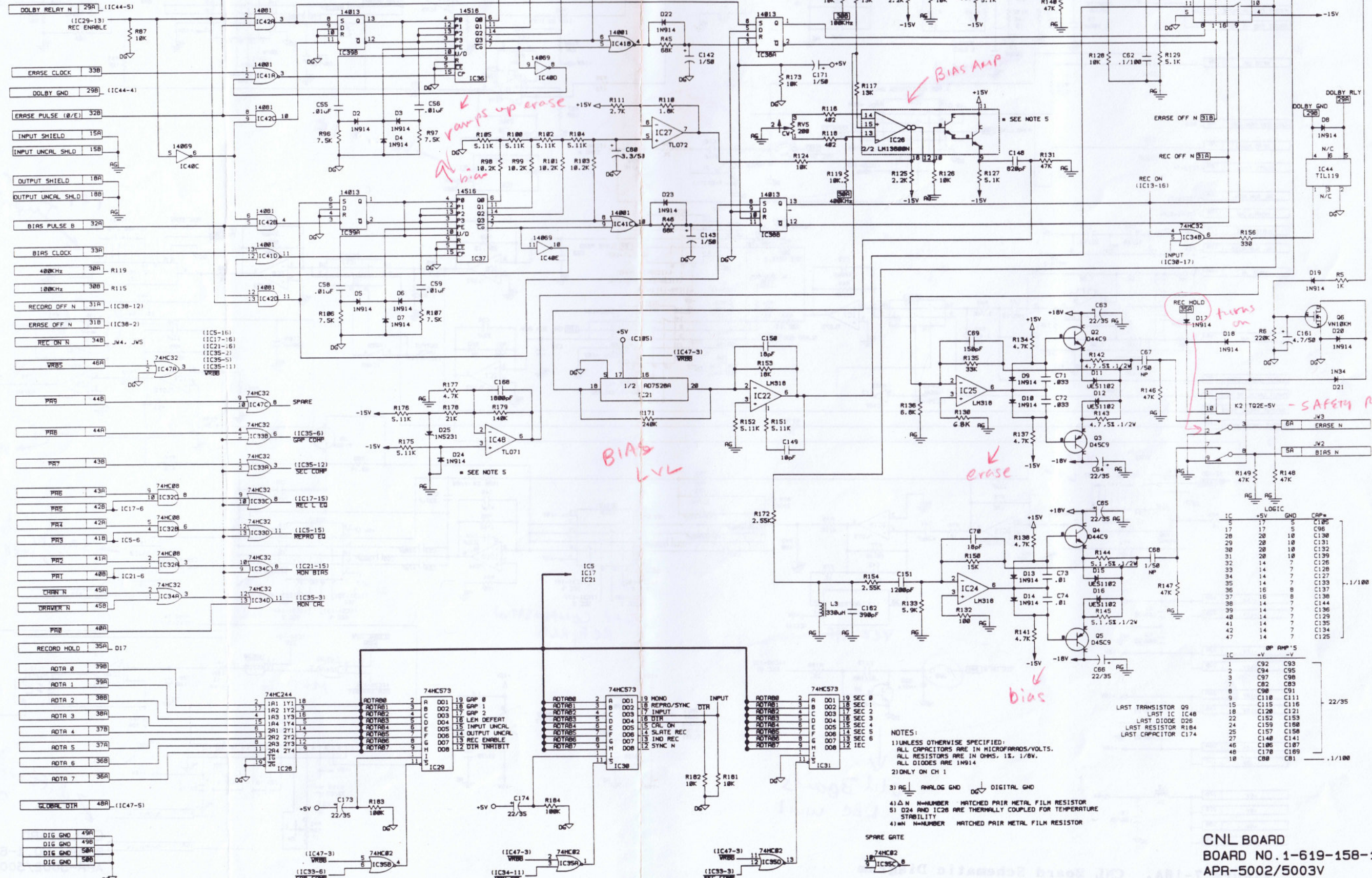


Figure 7-10A. CNL Board Schematic Diagram

CNL BOARD
BOARD NO. 1-619-158-11 & HIGHER
APR-5002/5003V

CNL BOARD

ANALOG GND	1R
ANALOG GND	1B
ANALOG GND	2R
ANALOG GND	2B
ANALOG GND	3R
ANALOG GND	3B
ANALOG GND	4R
ANALOG GND	4B
ANALOG GND	AG

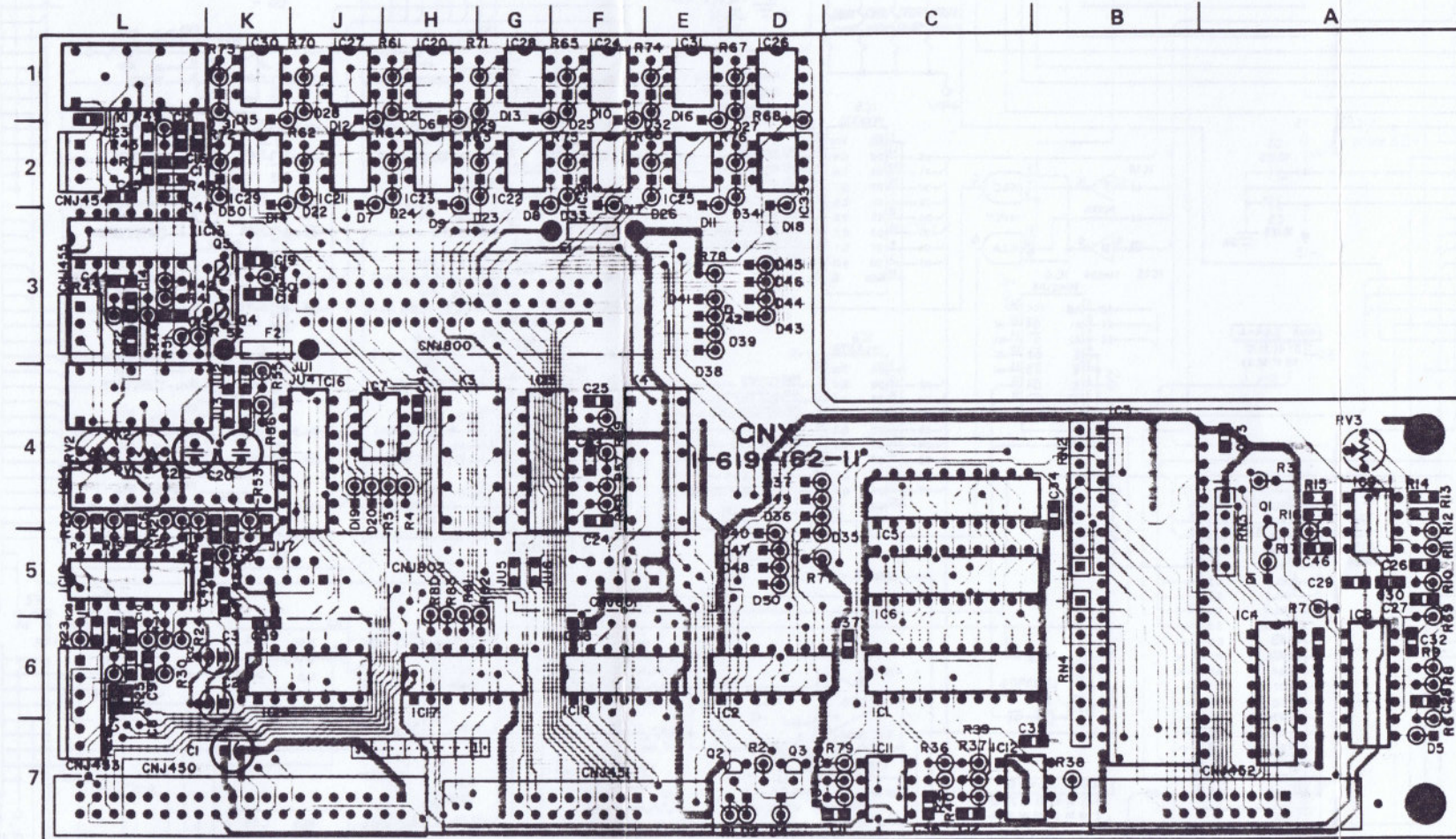


- NOTES:
- UNLESS OTHERWISE SPECIFIED: ALL CAPACITORS ARE IN MICROFARADS/VOLTS. ALL RESISTORS ARE IN OHMS, 1%, 1/8W. ALL DIODES ARE 1N914
 - ONLY ON CH 1
 - AG ANALOG GND DG DIGITAL GND
 - Δ N-NUMBER MATCHED PAIR METAL FILM RESISTOR
 - D24 AND IC26 ARE THERMALLY COUPLED FOR TEMPERATURE STABILITY
 - N N-NUMBER MATCHED PAIR METAL FILM RESISTOR
- SPARE GATE
- | | | | |
|----|------|------|-----|
| IC | +V | -V | CAP |
| 1 | C92 | C93 | |
| 2 | C94 | C95 | |
| 3 | C97 | C98 | |
| 4 | C82 | C83 | |
| 5 | C90 | C91 | |
| 6 | C118 | C119 | |
| 7 | C115 | C116 | |
| 8 | C120 | C121 | |
| 9 | C152 | C153 | |
| 10 | C159 | C160 | |
| 11 | C157 | C158 | |
| 12 | C148 | C149 | |
| 13 | C186 | C187 | |
| 14 | C170 | C169 | |
| 15 | C80 | C81 | |

CNL BOARD
BOARD NO. 1-619-158-11 & HIGHER
APR-502/503V

Figure 7-10B CNL Board Schematic Diagram

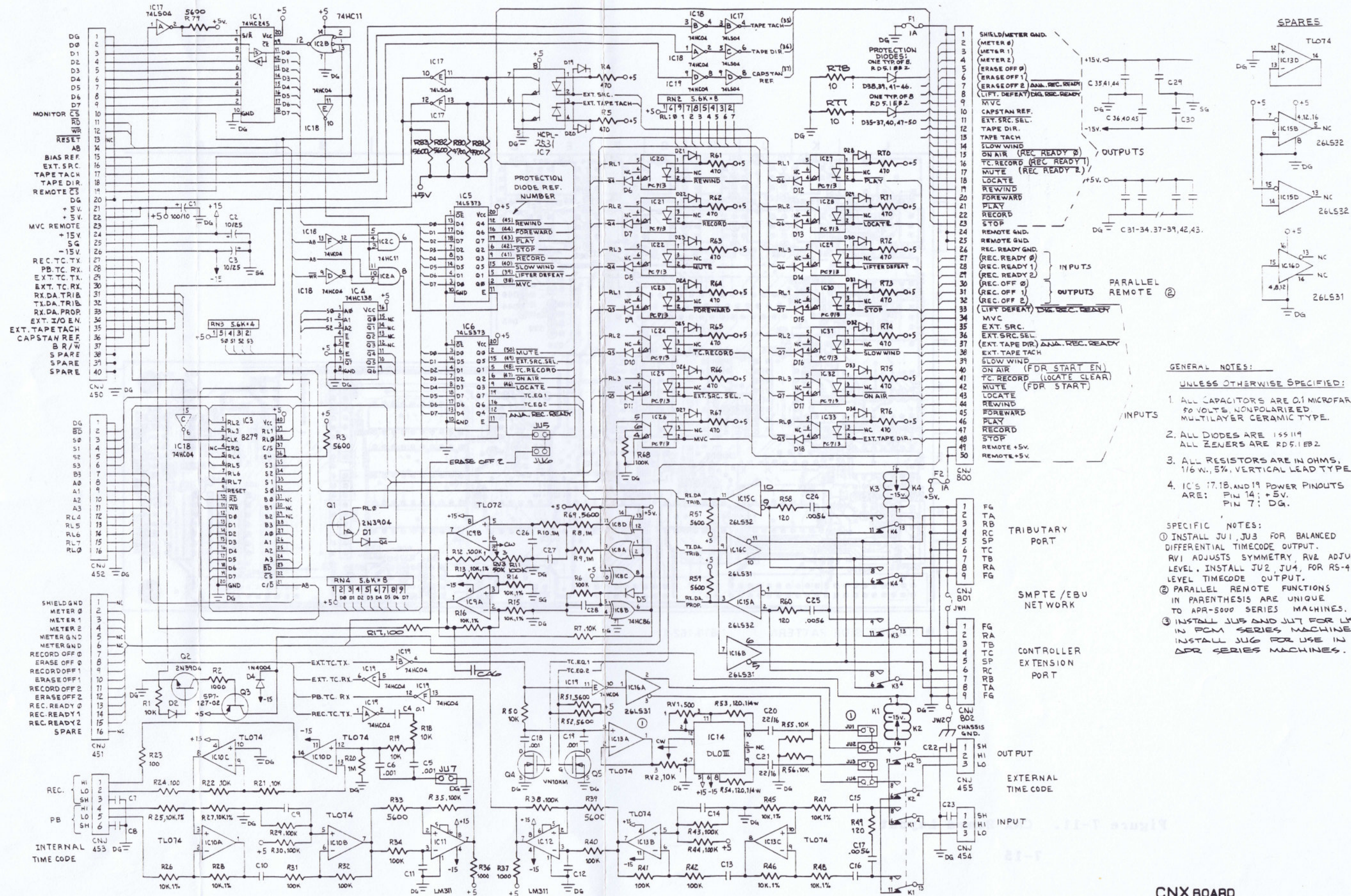
CNX BOARD (1-619-162-11)
Component Side



■ SOLDER SIDE PATTERN 1-619-162-11

Figure 7-11. CNX Board Layout

CNX BOARD



- GENERAL NOTES:**
1. ALL CAPACITORS ARE 0.1 MICROFARAD, 50 VOLTS, NONPOLARIZED MULTILAYER CERAMIC TYPE.
 2. ALL DIODES ARE 1SS119 ALL ZENERS ARE RD5.1EB2
 3. ALL RESISTORS ARE IN OHMS, 1/6 W., 5%, VERTICAL LEAD TYPE.
 4. IC'S 17, 18, AND 19 POWER PINOUTS ARE: PIN 14; +5V. PIN 7; DG.

- SPECIFIC NOTES:**
1. INSTALL J1, J3 FOR BALANCED DIFFERENTIAL TIMECODE OUTPUT. RV1 ADJUSTS SYMMETRY, RV2 ADJUSTS LEVEL. INSTALL J2, J4, FOR RS-422 LEVEL TIMECODE OUTPUT.
 2. PARALLEL REMOTE FUNCTIONS IN PARENTHESIS ARE UNIQUE TO APR-5000 SERIES MACHINES.
 3. INSTALL J15 AND J17 FOR USE IN PCM SERIES MACHINES. INSTALL J16 FOR USE IN DDR SERIES MACHINES.

Figure 7-12. CNX Board Schematic Diagram

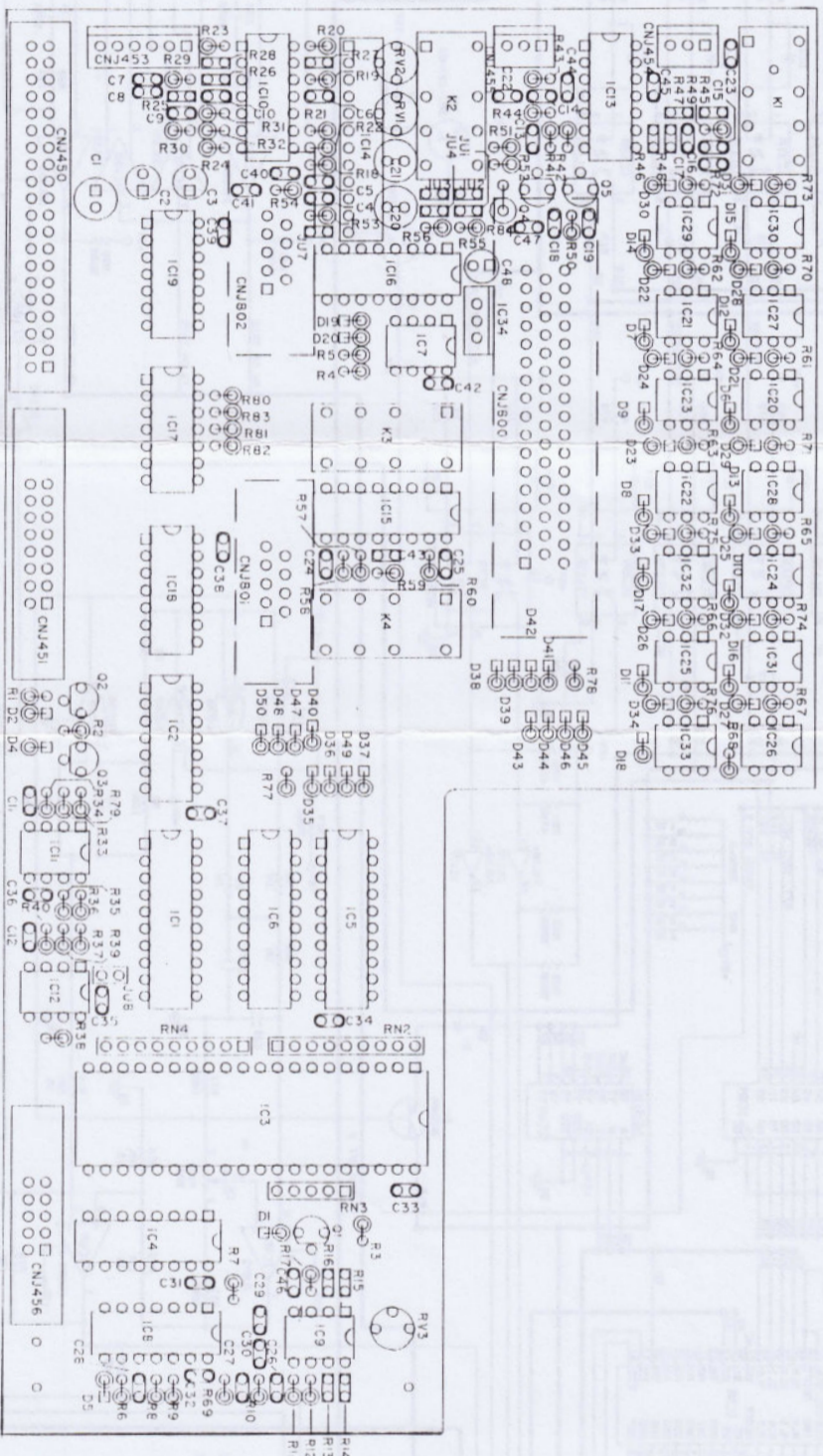


Figure 7-13. CNX-II Board Layout

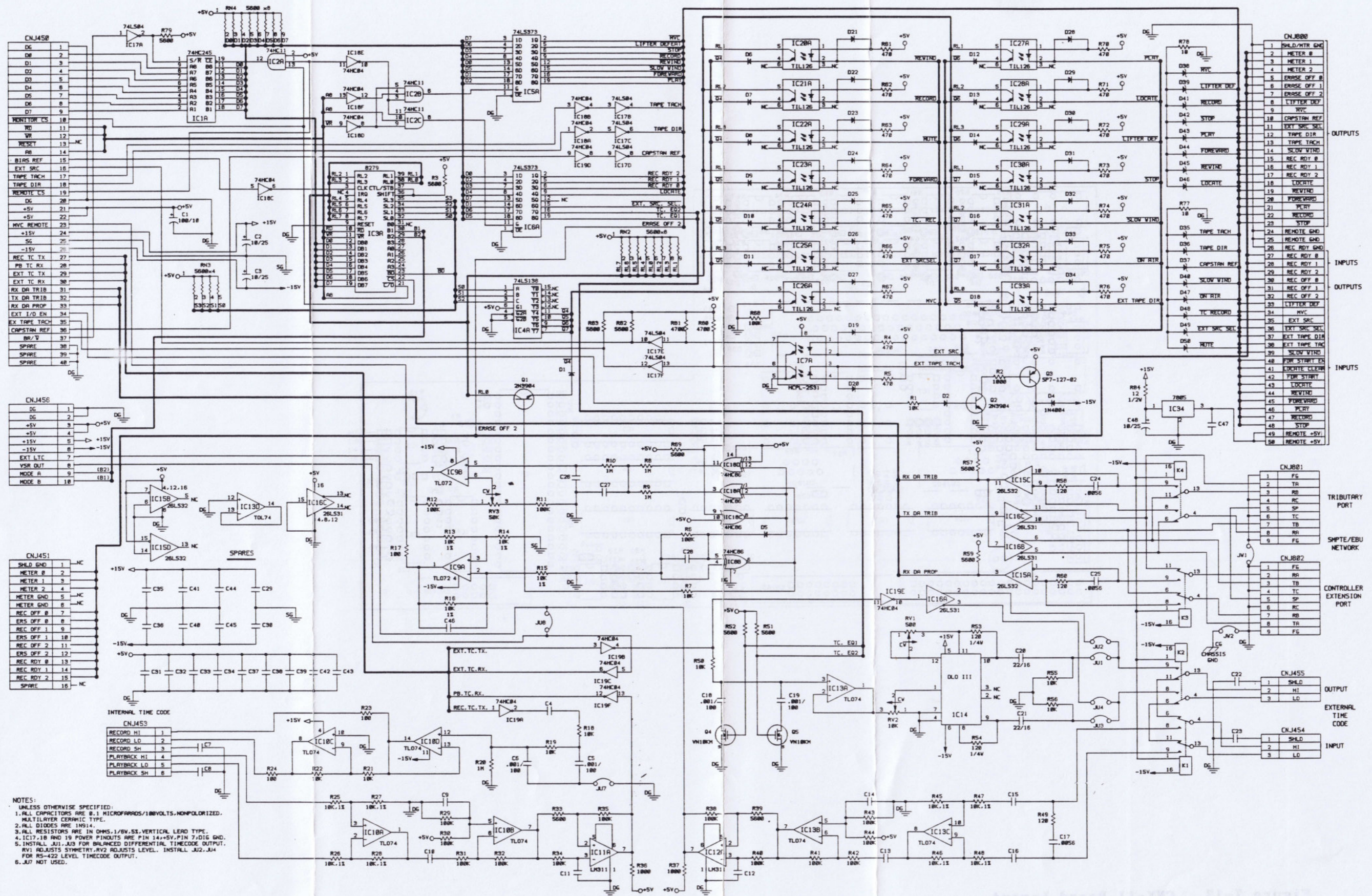
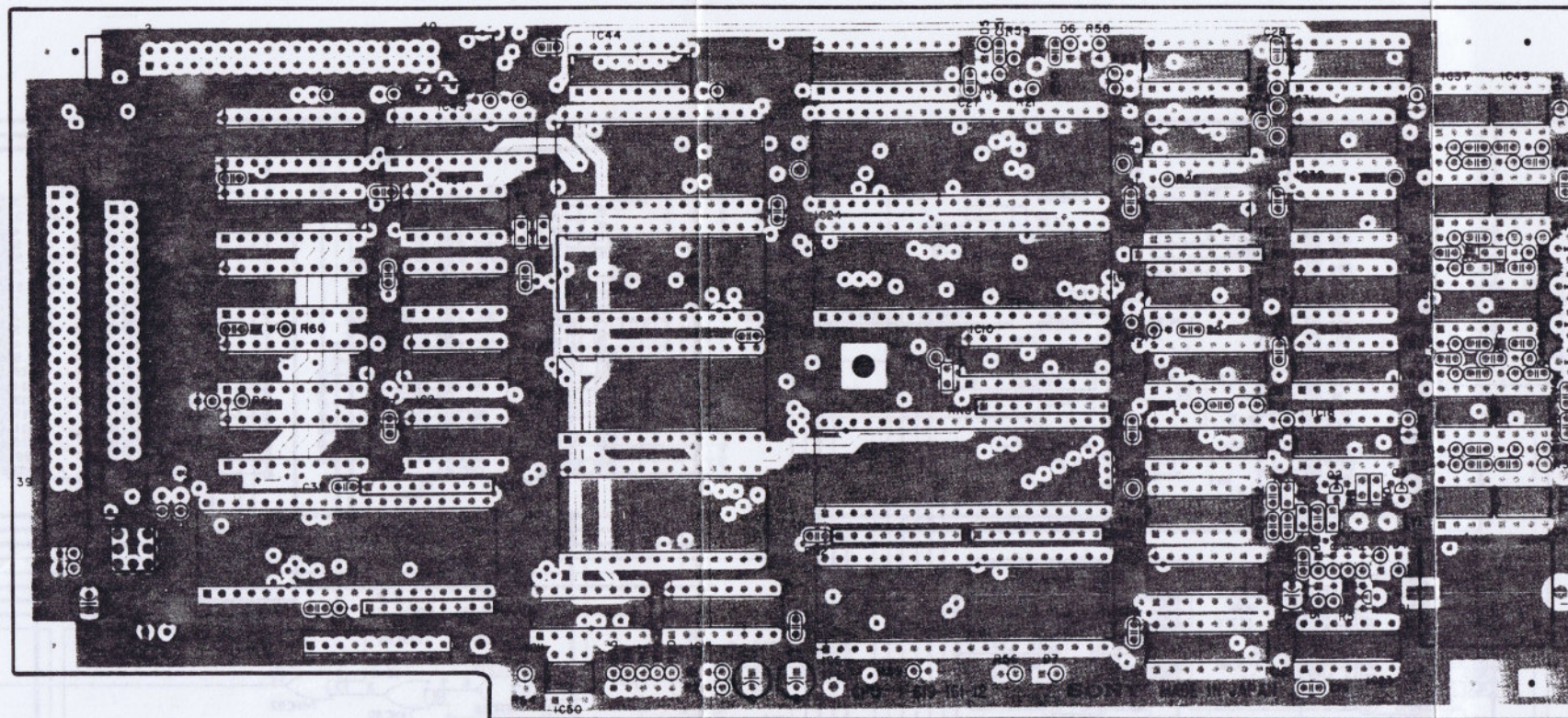
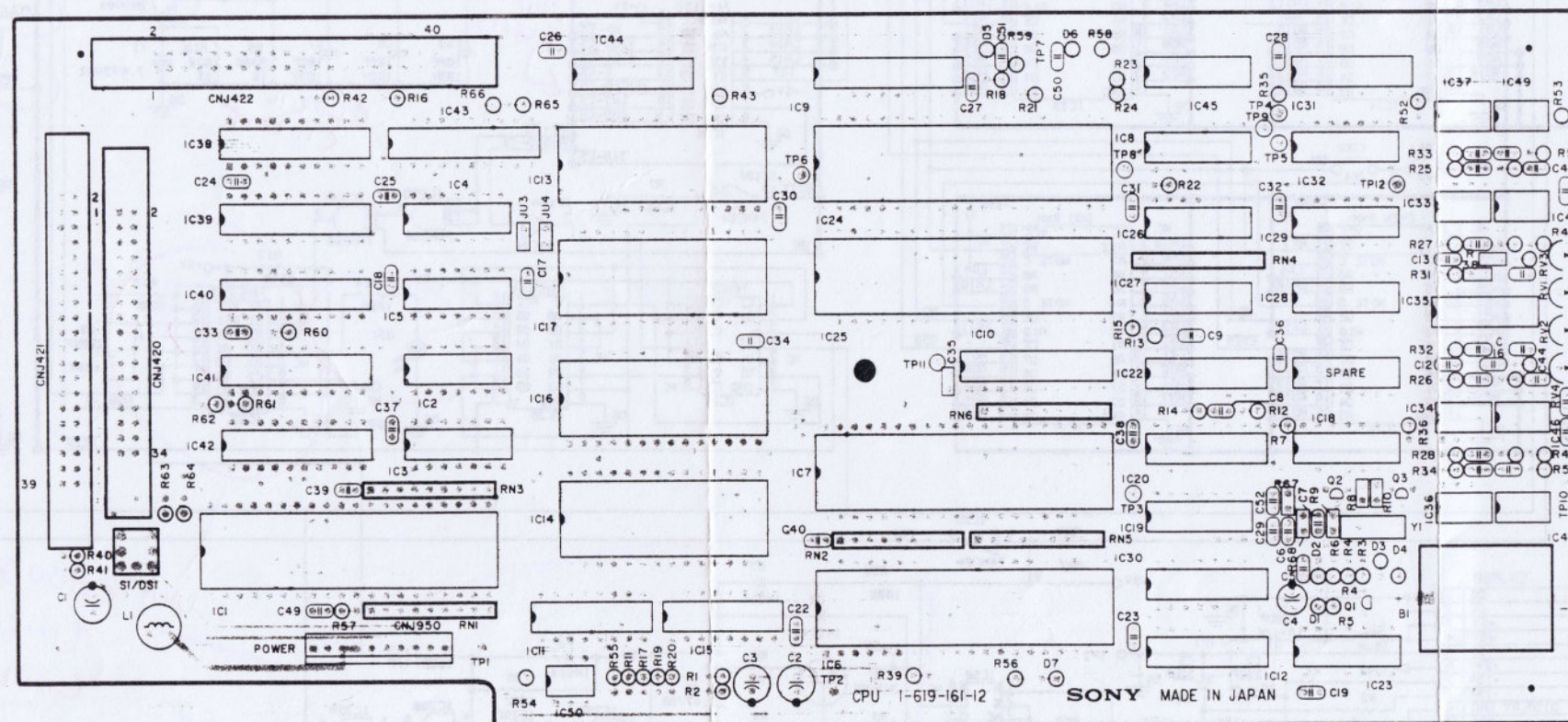


Figure 7-14. CNX-II Schematic Diagram

CPU BOARD (1-619-161-12)
Component Side



■ SOLDER SIDE PATTERN



■ SOLDER SIDE PATTERN

Figure 7-15. CPU Board Layout

CPU BOARD

Main Unit CPU (1/3) CPU (1/3) Main Unit

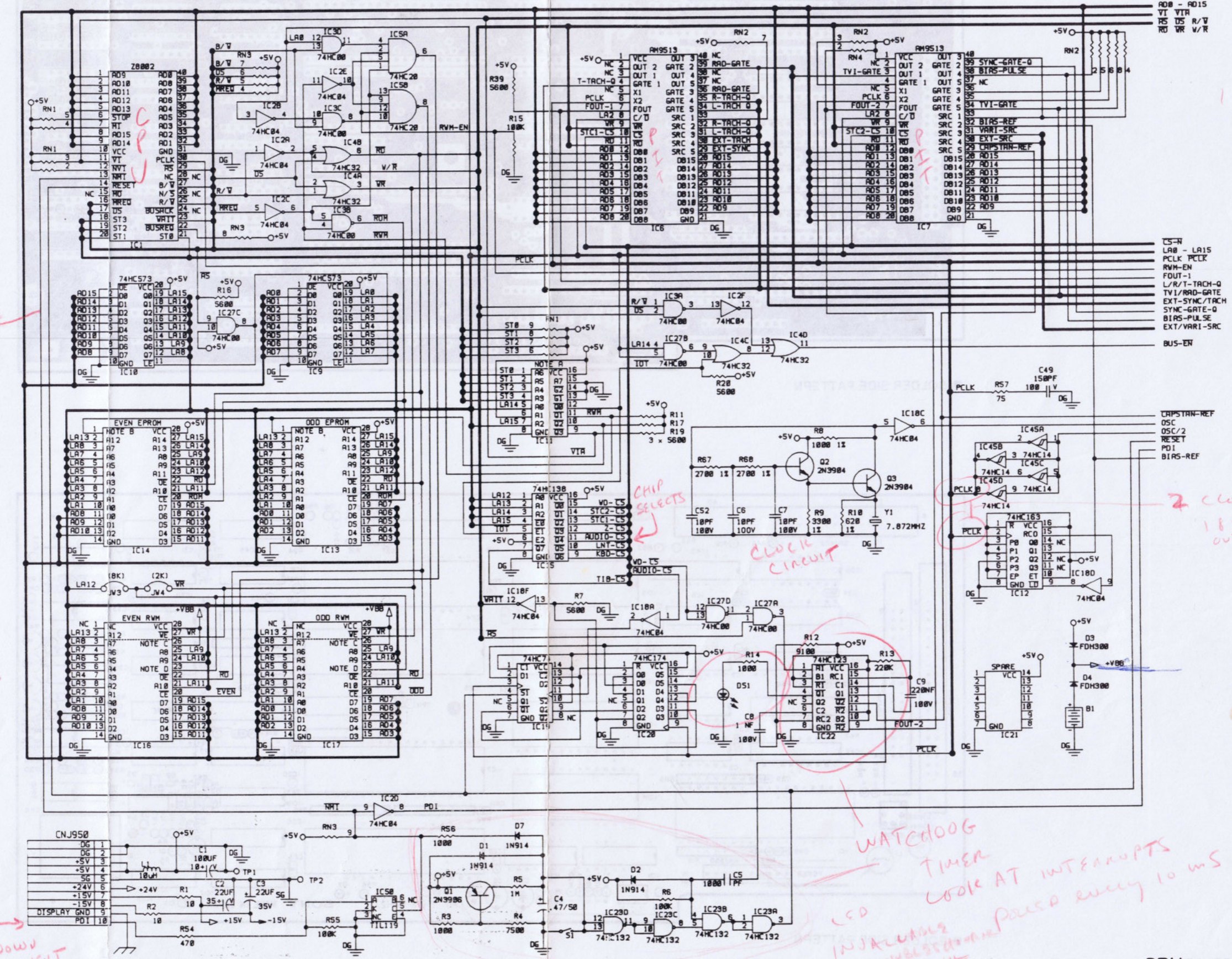
PIT Programmable Interrupt (CHANGE FAILED)

Address Latches

Ram

Passes STARD RAM

From PS PDI = Power Down Imminent



IC 15 HAS FAILURE

CHIP SELECTS

CLOCK CIRCUIT

2 clocks 180° out of phase

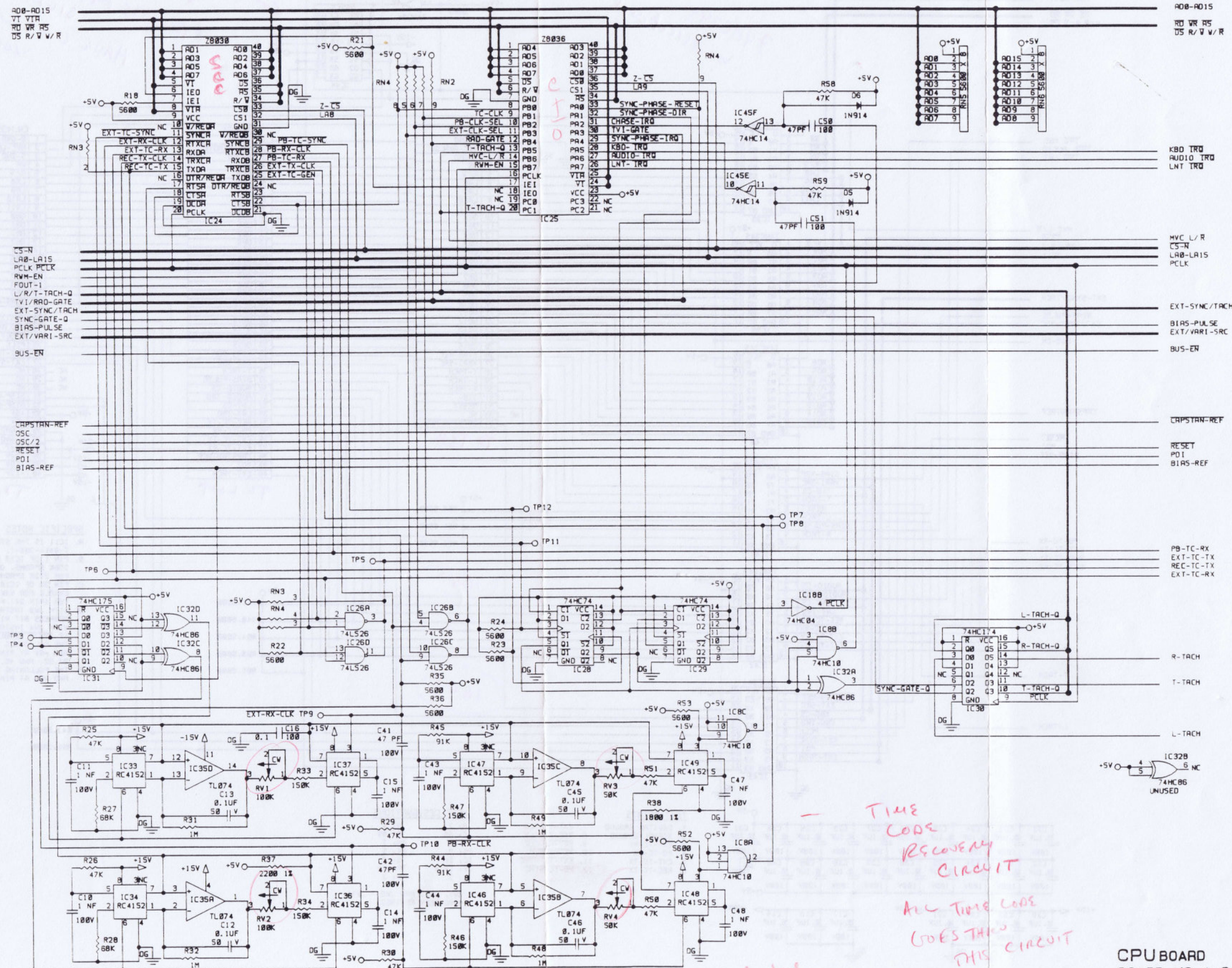
WATCHDOG

TIMER
LOOK AT INTERRUPTS
LCD
INJALABLE
POWER SUPPLY 10ms
WHS-CIT
CAS LOCKED

Figure 7-16A. CPU Board Schematic Diagram

CPU BOARD

See = Serial Communication Controller may not exist on TC unit -

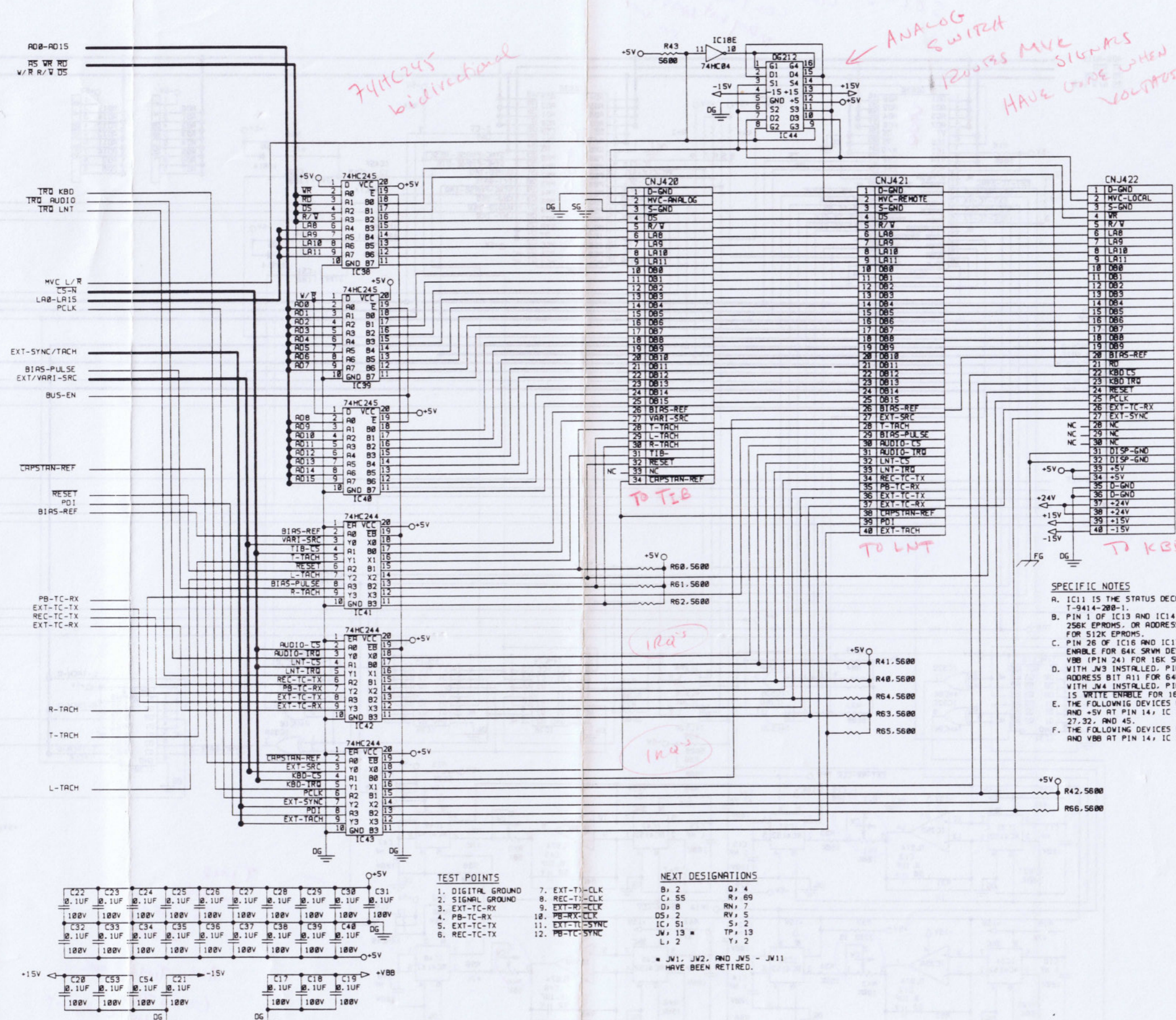


TIME CODE RECOVERY CIRCUIT ALL TIME CODE DOES THROUGH THIS CIRCUIT

IF misadjusted unit requires TC

Figure 7-16B. CPU Board Schematic Diagram

CPU BOARD

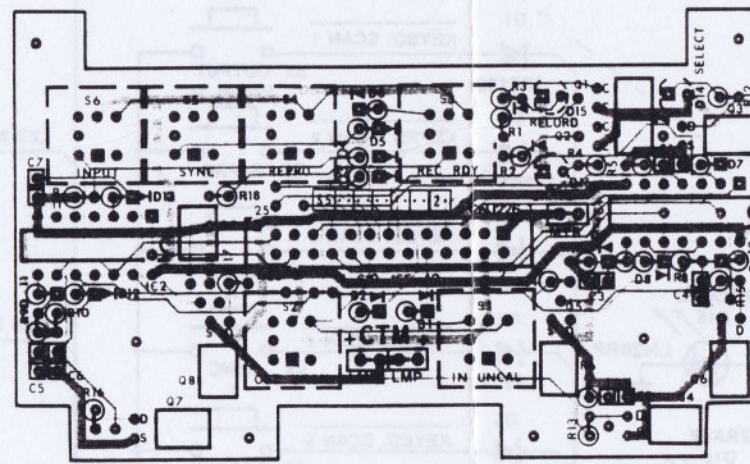


- SPECIFIC NOTES**
- A. IC11 IS THE STATUS DECODER PROM. T-9414-200-1.
 - B. PIN 1 OF IC13 AND IC14 IS VPP FOR 256K EPROMS, OR ADDRESS BIT A15 FOR 512K EPROMS.
 - C. PIN 26 OF IC16 AND IC17 IS CHIP ENABLE FOR 64K SRAM DEVICES, OR VBB (PIN 24) FOR 16K SRAM DEVICES.
 - D. WITH JW3 INSTALLED, PIN 23 IS ADDRESS BIT A11 FOR 64K SRAM DEVICES. WITH JW4 INSTALLED, PIN 23 (PIN 21) IS WRITE ENABLE FOR 16K SRAM DEVICES.
 - E. THE FOLLOWING DEVICES HAVE DG AT PIN 7 AND +5V AT PIN 14; IC 2,3,4,8,18,26, 27,32, AND 45.
 - F. THE FOLLOWING DEVICES HAVE DG AT PIN 7 AND VBB AT PIN 14; IC 5,23.

Figure 7-16C. CPU Board Schematic Diagram

CTM Main Unit

CTM BOARD (1-619-165-12)
Component Side



■ SOLDER SIDE PATTERN 1-619-165-12

Figure 7-17. CTM Board Layout

CTM BOARD

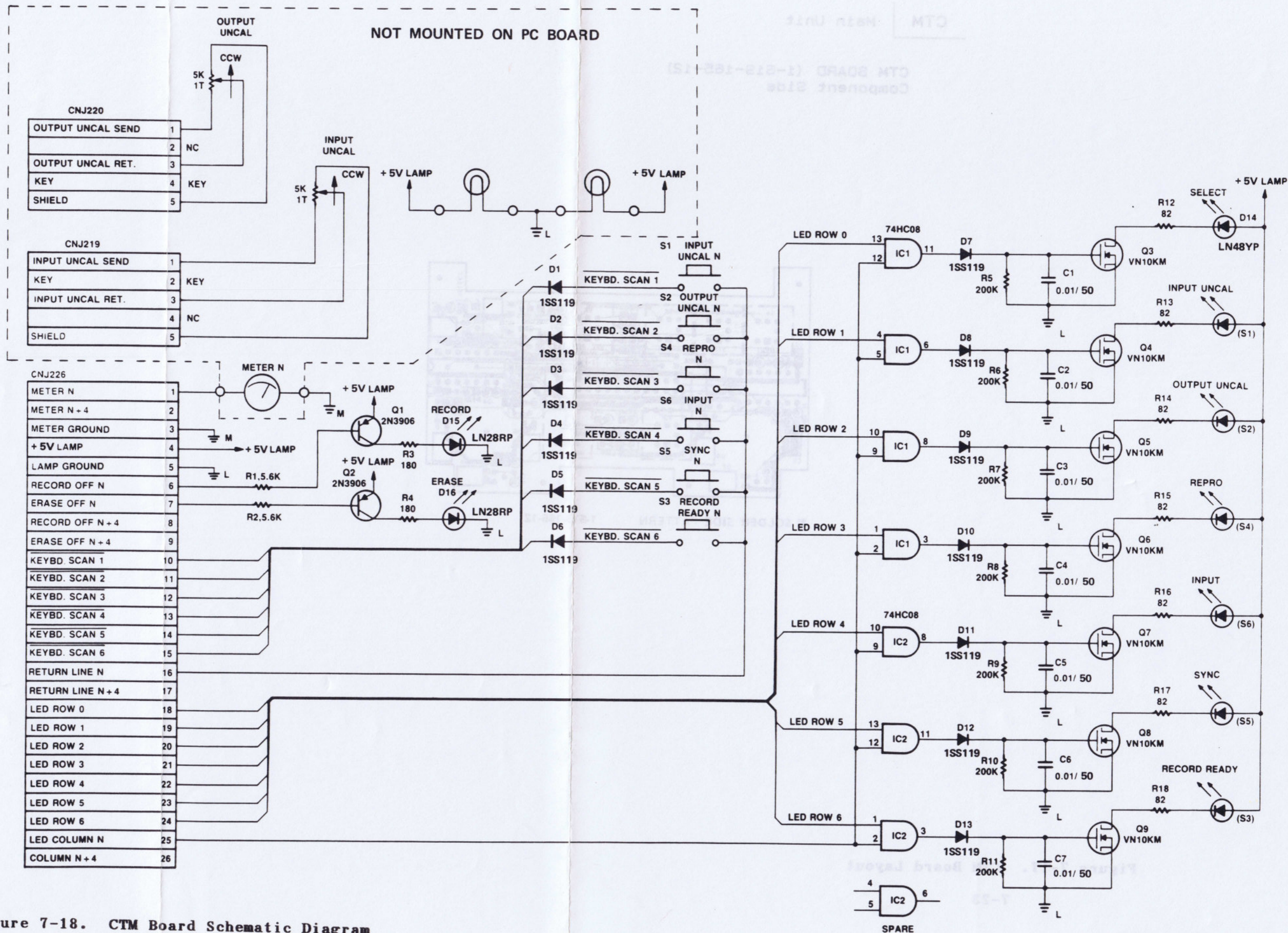


Figure 7-18. CTM Board Schematic Diagram

DSP BOARD (1-619-170-11)
Component Side

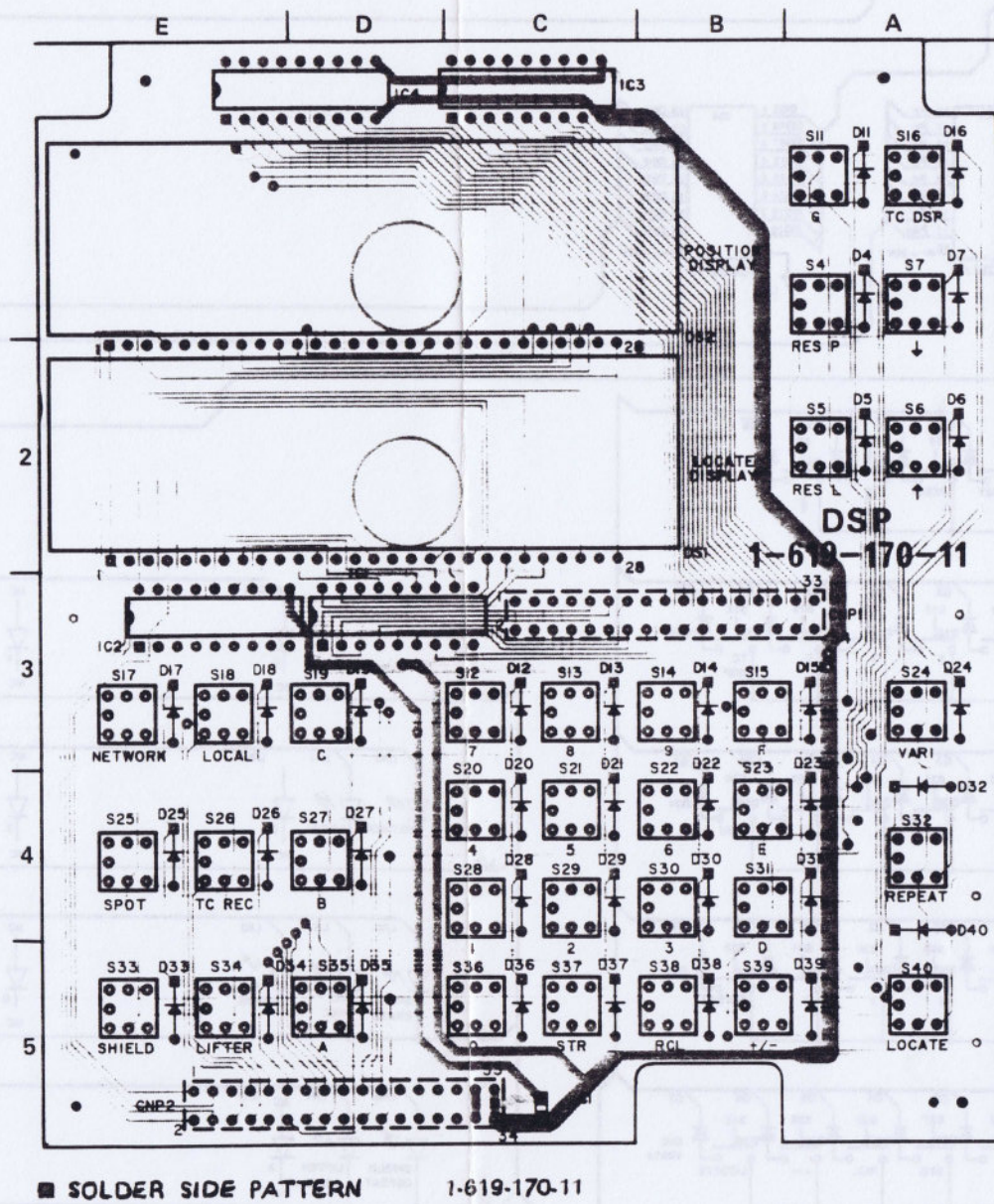
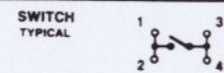
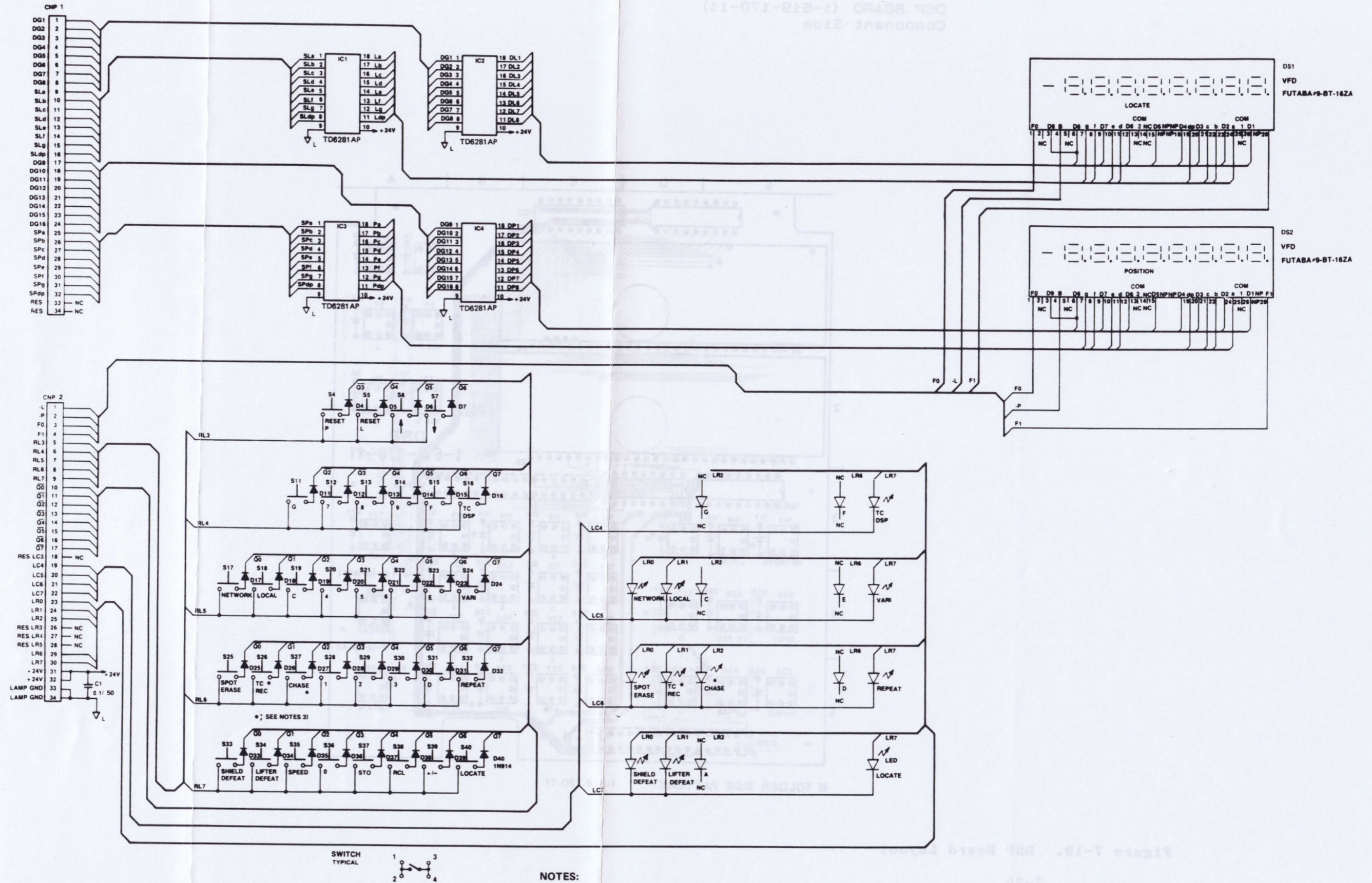


Figure 7-19. DSP Board Layout

DSP BOARD



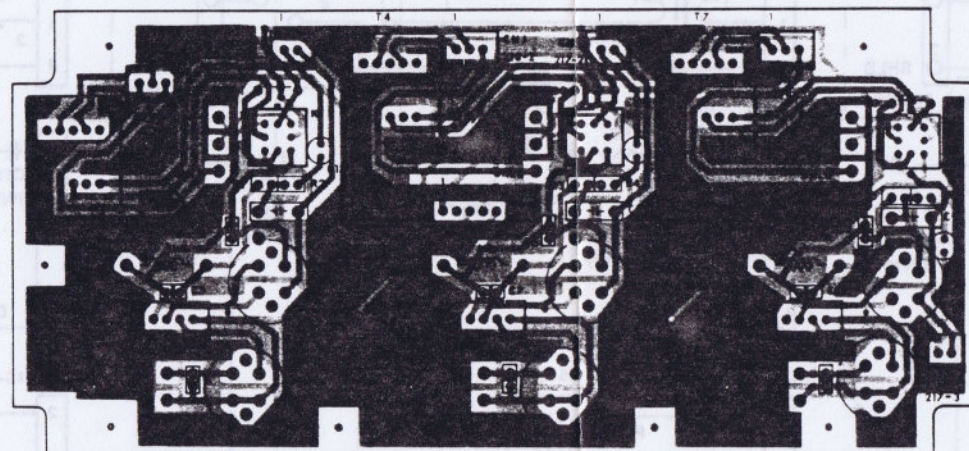
NOTES:

- 1) SWITCHES S11, S15, S19, S23 and S31 are not used.
- 2) DIODES D11, D15, D19, D23 and D31 are not used.
- 3) * S26, S27, D26 and D27 are installed in APR-5003, but not installed in APR-5002.

Figure 7-20. DSP Board Schematic Diagram

FEX BOARD (1-619-179-11)
Component Side

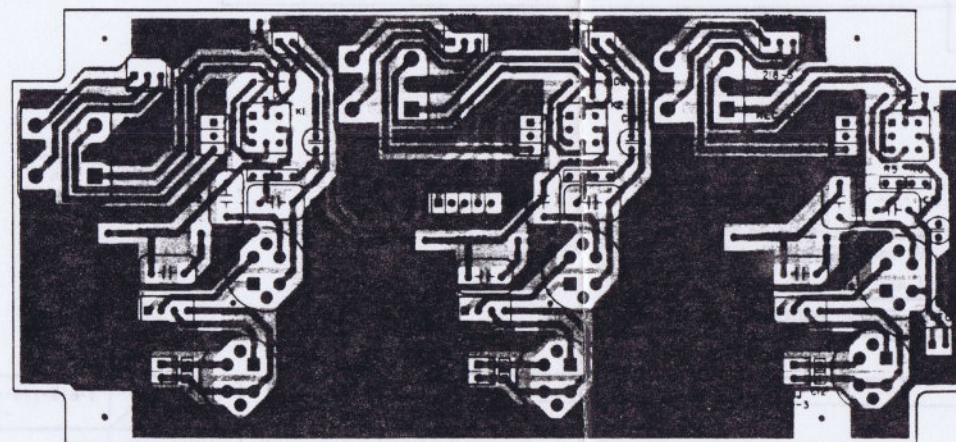
S/N; APR-5002 20001 TO 20300



■ SOLDER SIDE PATTERN 1-619-179-11

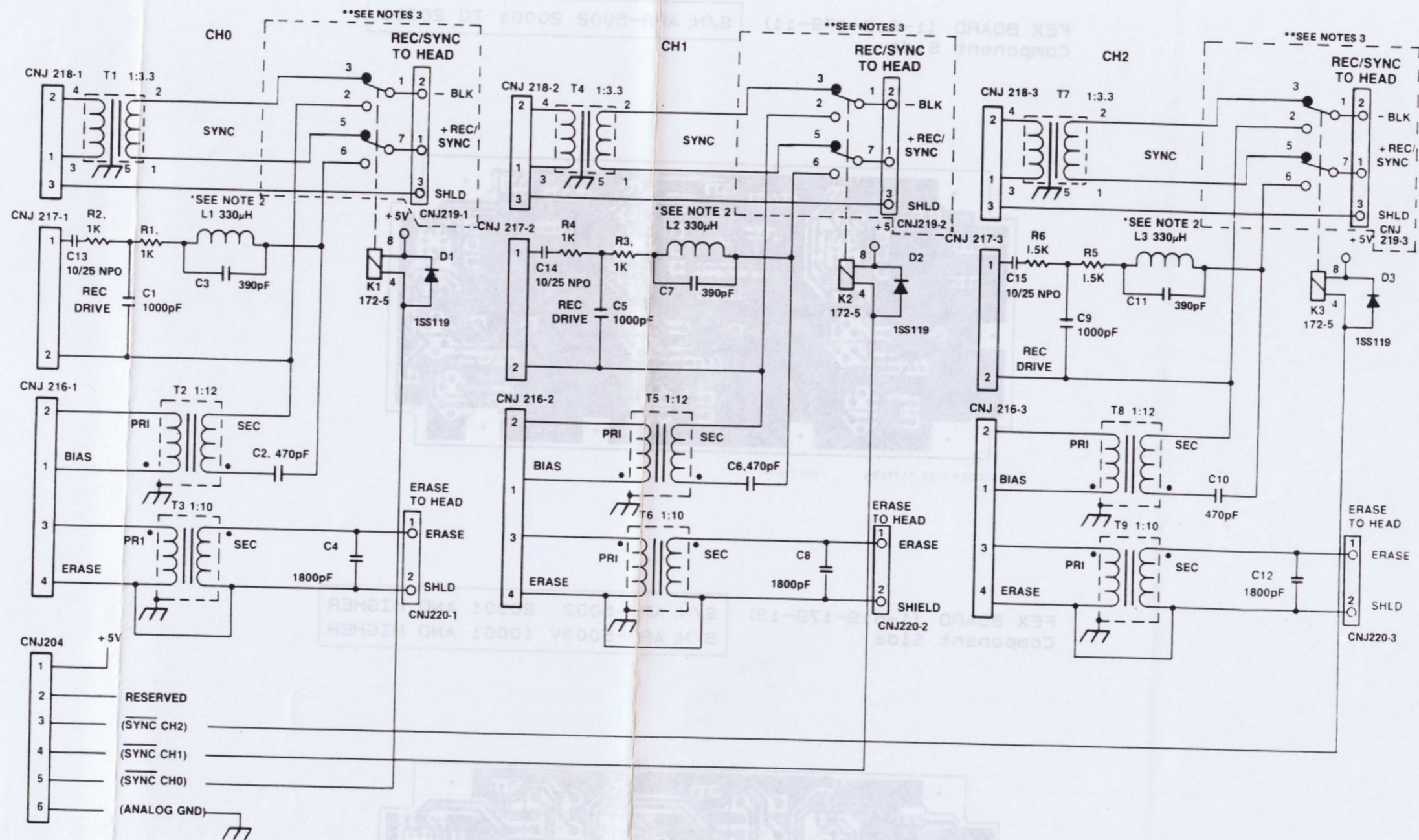
FEX BOARD (1-619-179-13)
Component Side

S/N; APR-5002 20301 AND HIGHER
S/N; APR-5003V 10001 AND HIGHER



■ SOLDER SIDE PATTERN 1-619-179-13

Figure 7-21. FEX Board Layout (Early and Late Model)

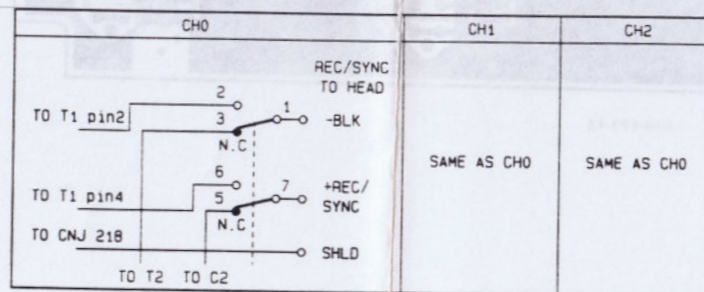


NOTES (UNLESS OTHERWISE SPECIFIED):

- 1. ALL RESISTOR VALUES ARE IN OHMS, 1/8 W. 1%.
- 2. L1, L2 & L3 ARE SHIELDED BY WRAPPING EACH INDUCTOR WITH μ METAL, THEN INCAPSULATE THE WRAPPED INDUCTOR IN SHRINK TUBING.

**3. The following circuit is only applicable to the FEX Board (Board No. 1-619-179-11 and -12 only).

Serial Nos:
 APR-5002 20001 TO 20300

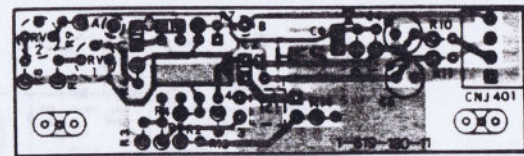


FEX CNL. TCC	1-619-179-11 -12	1-619-179-13 and higher
1-619-158-11 -12	No Problem	Can't use
1-619-158-13 and higher	Add: JW4 Q9 (P1086) Delete: JW5	Add: JW5 Delete: Q9 and JW4

Applicable Serial NO.		Parts that have been changed.	Pins that have been changed.	Parts that have been added.
APR-5002	APR-5003	C3, C7, C11 430pF \rightarrow 390pF		
20201 and higher	20401 and higher			
20301 and higher	20501 and higher	R1, R2, R3, R4 1.5K \rightarrow 1K	T1, T4, T7 8Pin \rightarrow 4Pin 6Pin \rightarrow 3Pin 4Pin \rightarrow 1Pin GND \rightarrow 5Pin	CNJ219 CNJ220

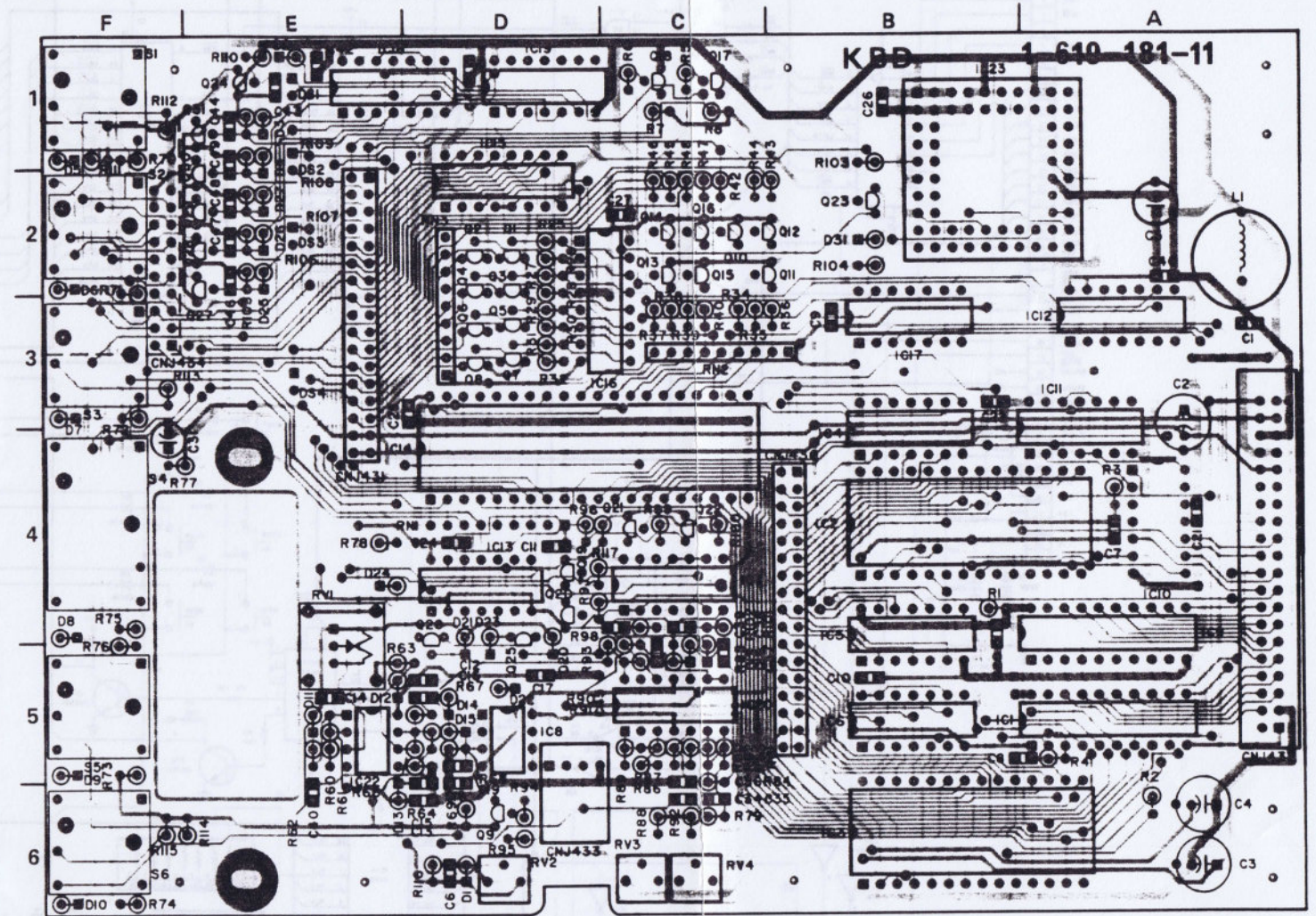
Figure 7-22. FEX Board Schematic Diagram

HES BOARD (1-619-180-11)
Component Side



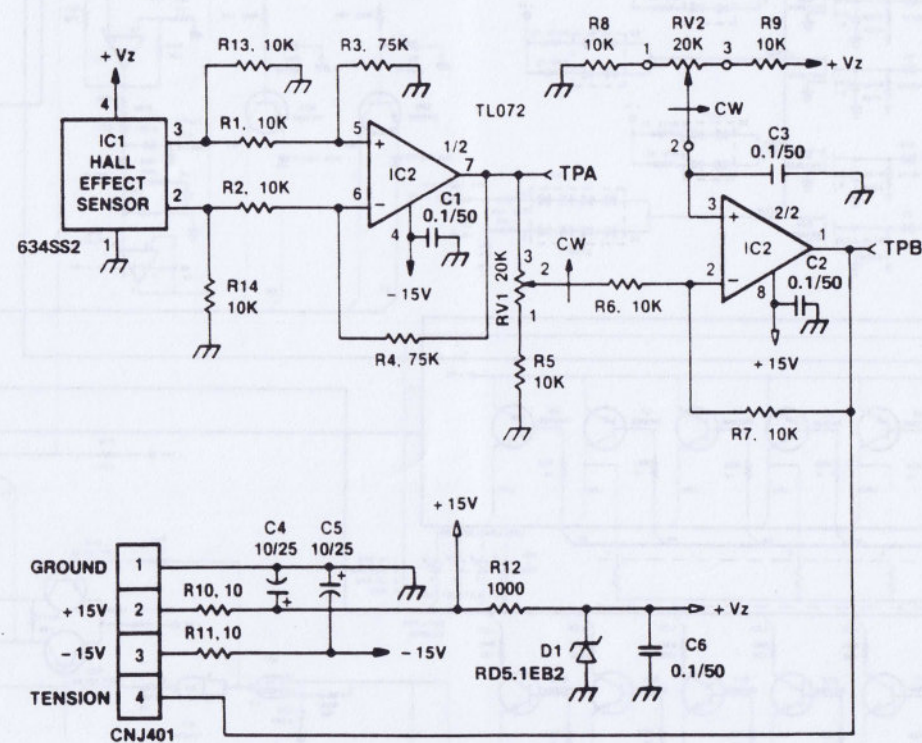
SOLDER SIDE PATTERN 1-619-180-11

KBD BOARD (1-619-181-11)
Component Side



SOLDER SIDE PATTERN 1-619-181-11

HES BOARD



NOTES: UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTOR VALUES ARE IN OHMS, 1/6W, 5%.
2. ALL CAPACITORS MEASURED IN MICROFARADS/VOLTS.
3. HALL EFFECT SENSOR IS 634SS2 OR EQUIVALENT.

HES BOARD
BOARD NO. 1-619-180-11 & HIGHER
APR-5002/5003V

Figure 7-23. HES Board Layout/Schematic Diagram and KBD Board Layout

KBD BOARD

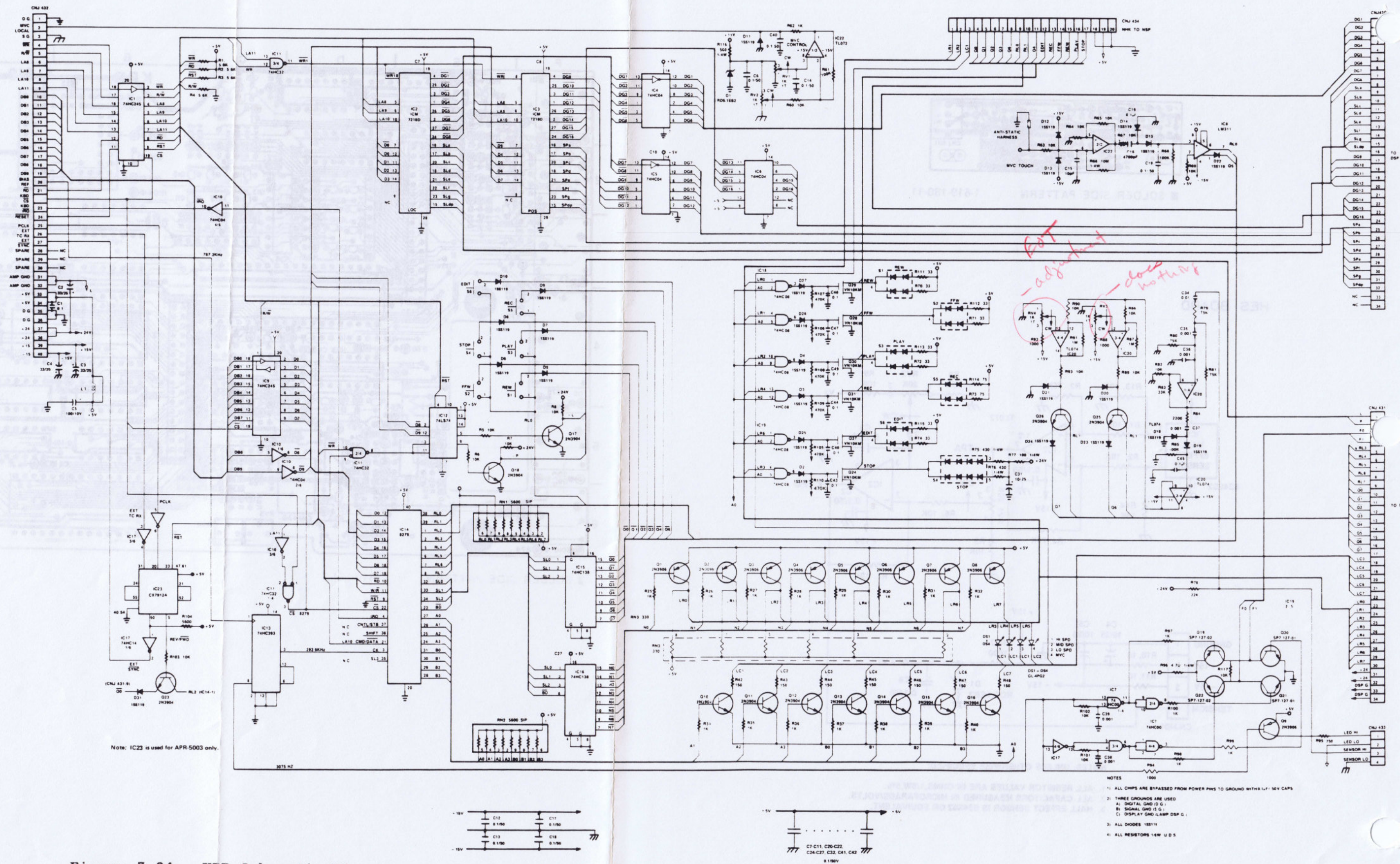
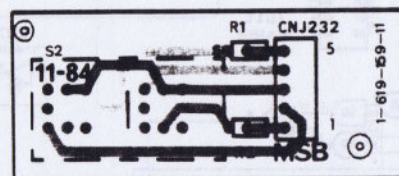


Figure 7-24. KBD Schematic Diagram

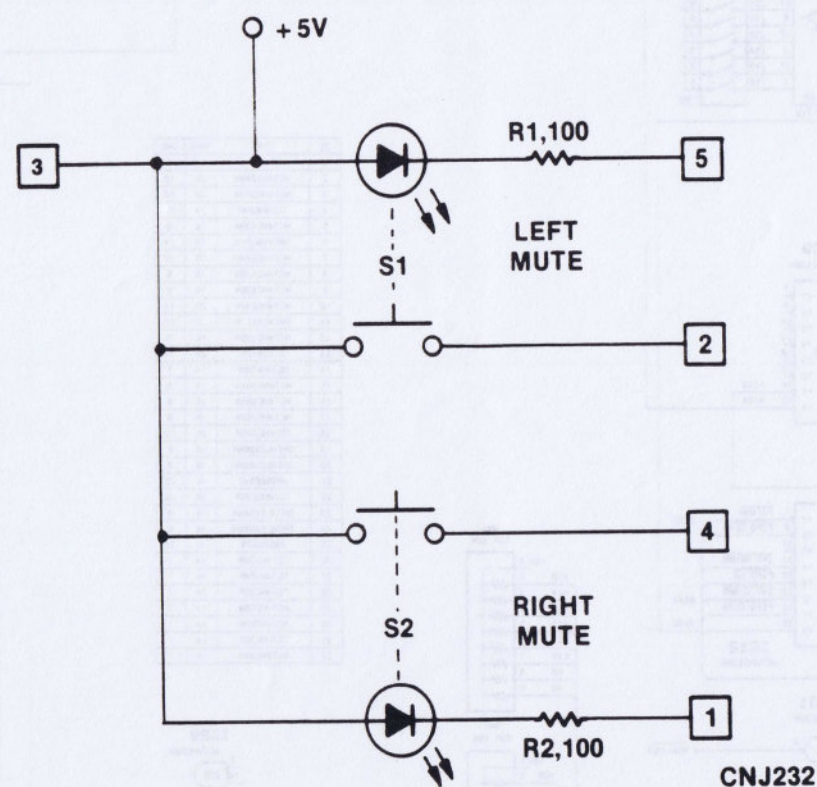
MSB BOARD (1-619-159-11)
Component Side

LNT BOARD (1-619-157-12)
Component Side

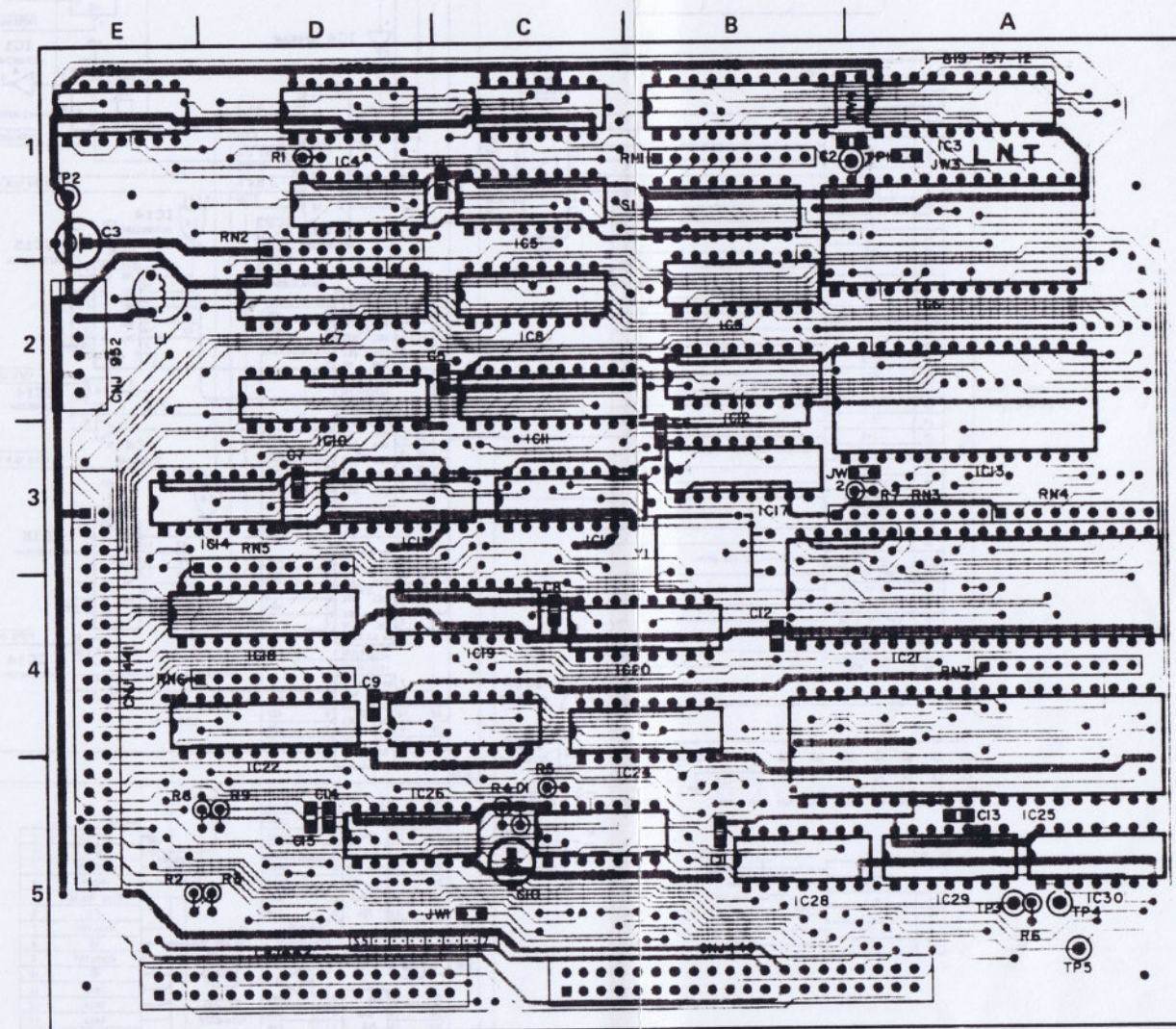


■ SOLDER SIDE PATTERN 1-619-159-11

MSB BOARD



NOTES(UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTOR VALUES ARE IN OHMS, 1/6W,5%



■ SOLDER SIDE PATTERN 1-619-157-12

Figure 7-25. MSB Board Layout/Schematic Diagram and LNT Board Layout

MSB BOARD
BOARD NO.1-619-159-11 & HIGHER
APR-5002/5003V

LNT BOARD

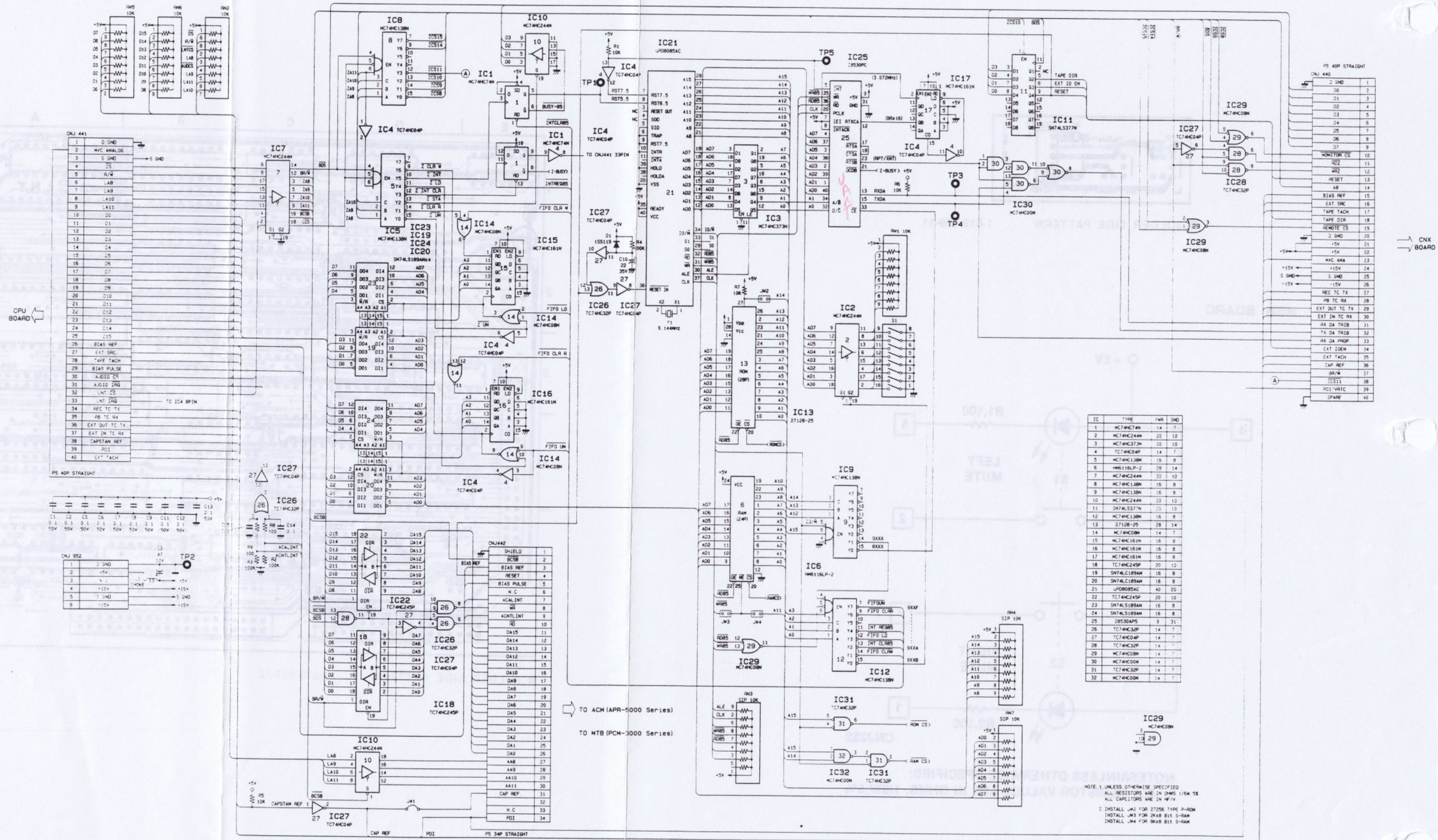
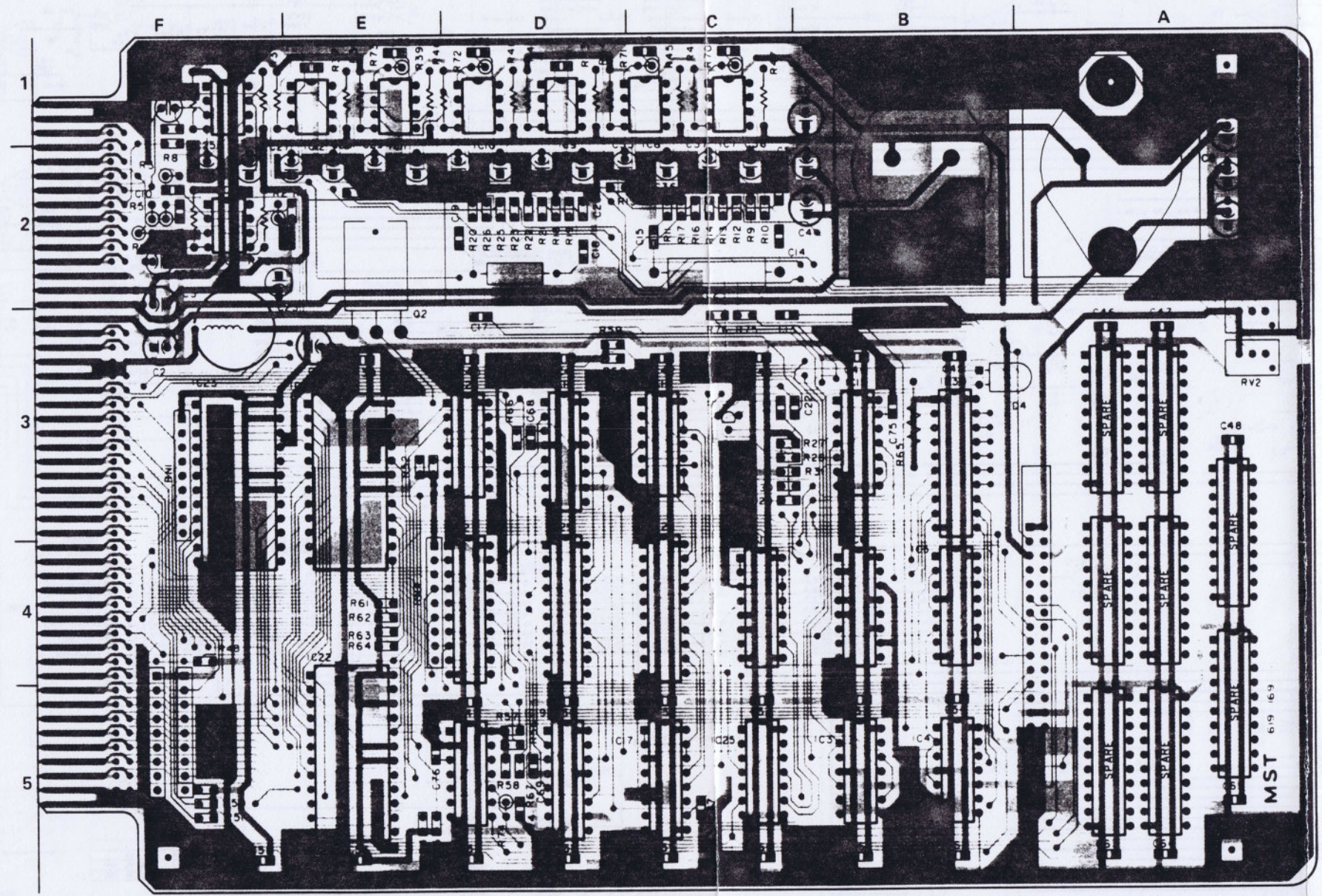


Figure 7-26. LNT Schematic Diagram

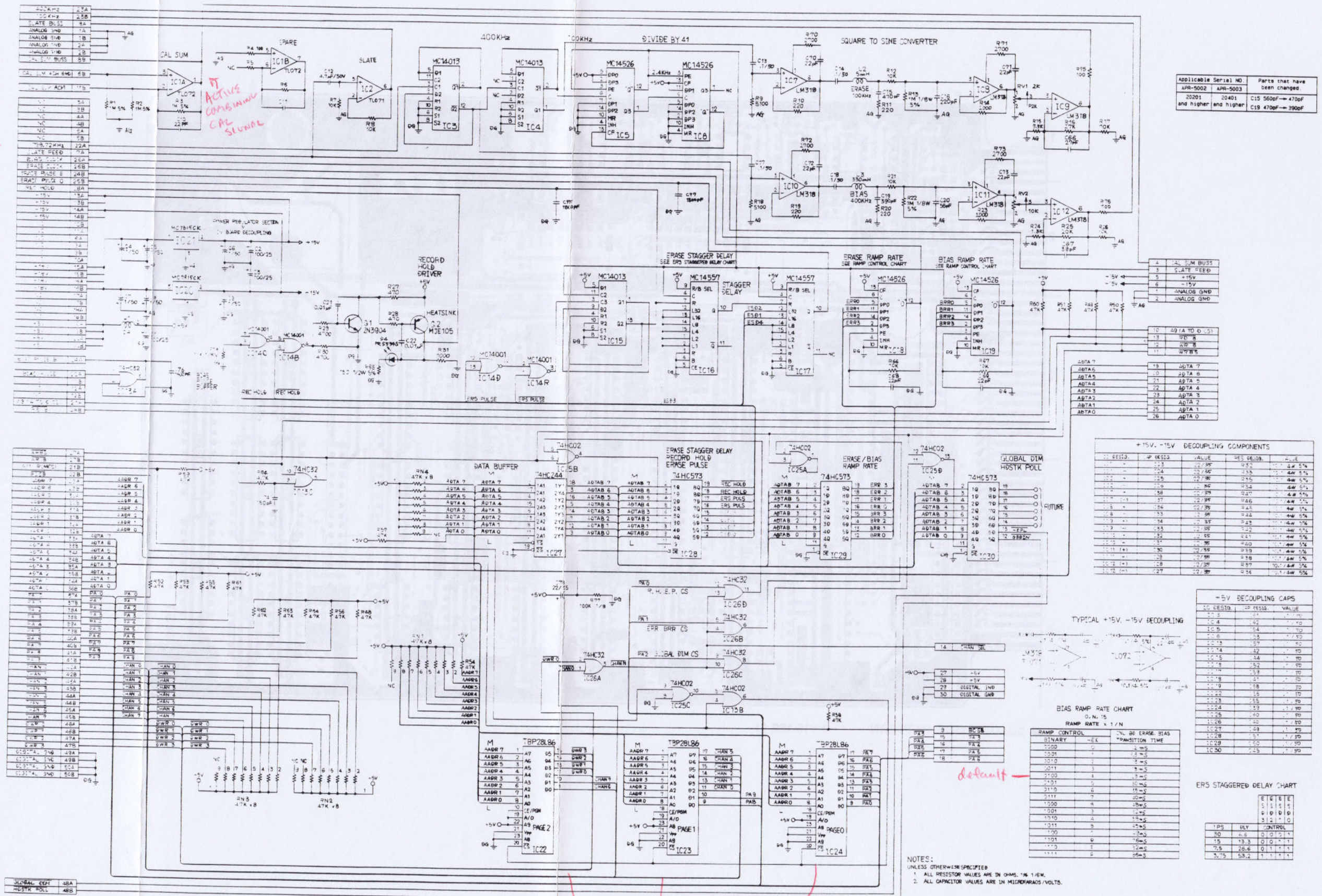
MST BOARD (1-619-169-11)
Component Side

S/N: APR-5002 20001 TO 20615



■ SOLDER SIDE PATTERN 1-619-169-11

Figure 7-27. MST Board Layout (Early Model)



798.72

+15V FROM PS

ACTIVE COMBINING CAP SIGNAL

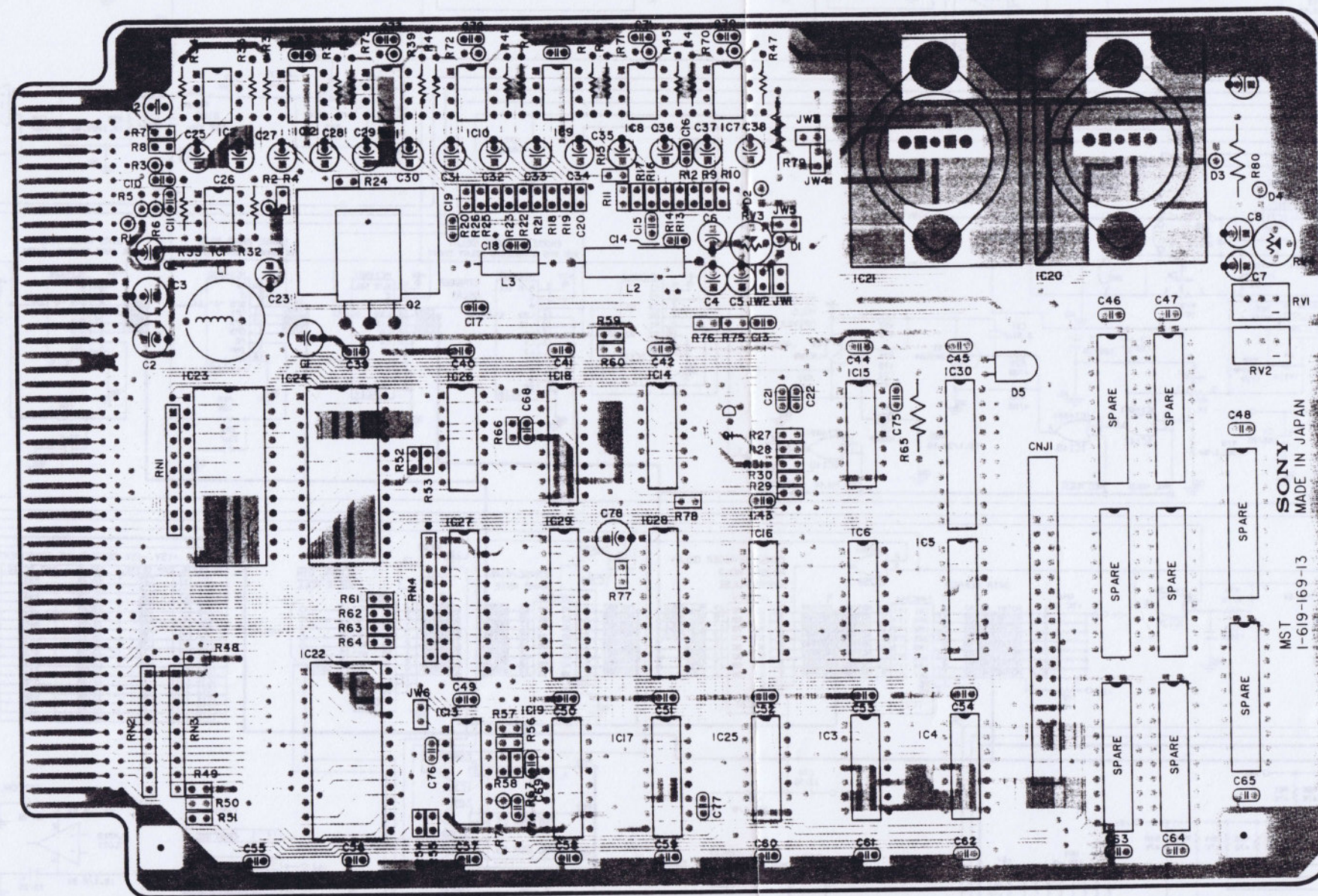
IDENTICAL PROMS

PA - PANAMETEK ADDRESS

Figure 7-28. MST Board Schematic Diagram (Early Model)

MST BOARD (1-619-169-13)
Component Side

S/N: APR-5002 20701 AND HIGHER
S/N: APR-5003V 10001 AND HIGHER



■ SOLDER SIDE PATTERN

Figure 7-29. MST Board Layout (Late Model)

MST BOARD (1-619-169-12 & HIGHER)

S/N: APR-5002 20701 AND HIGHER
S/N: APR-5003V 10001 AND HIGHER

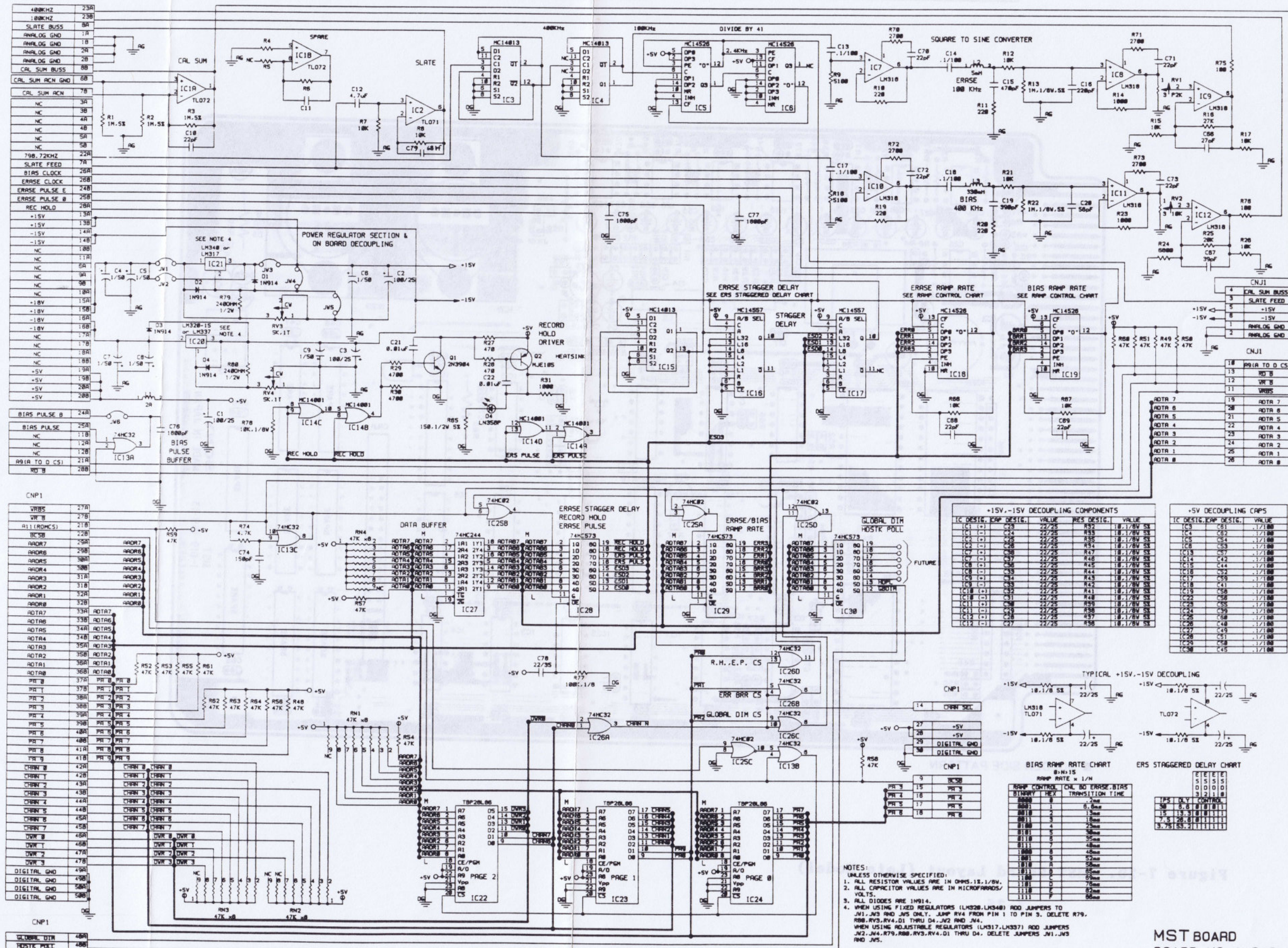
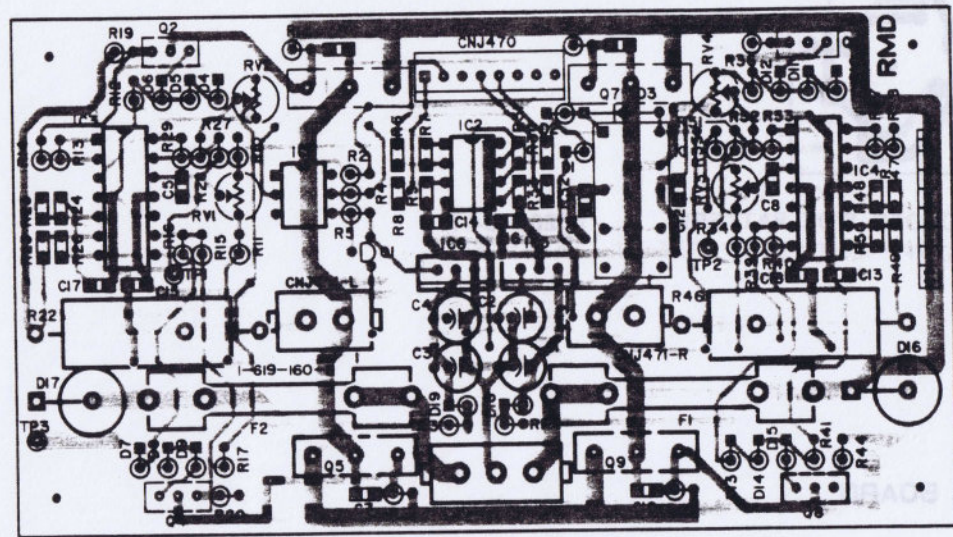
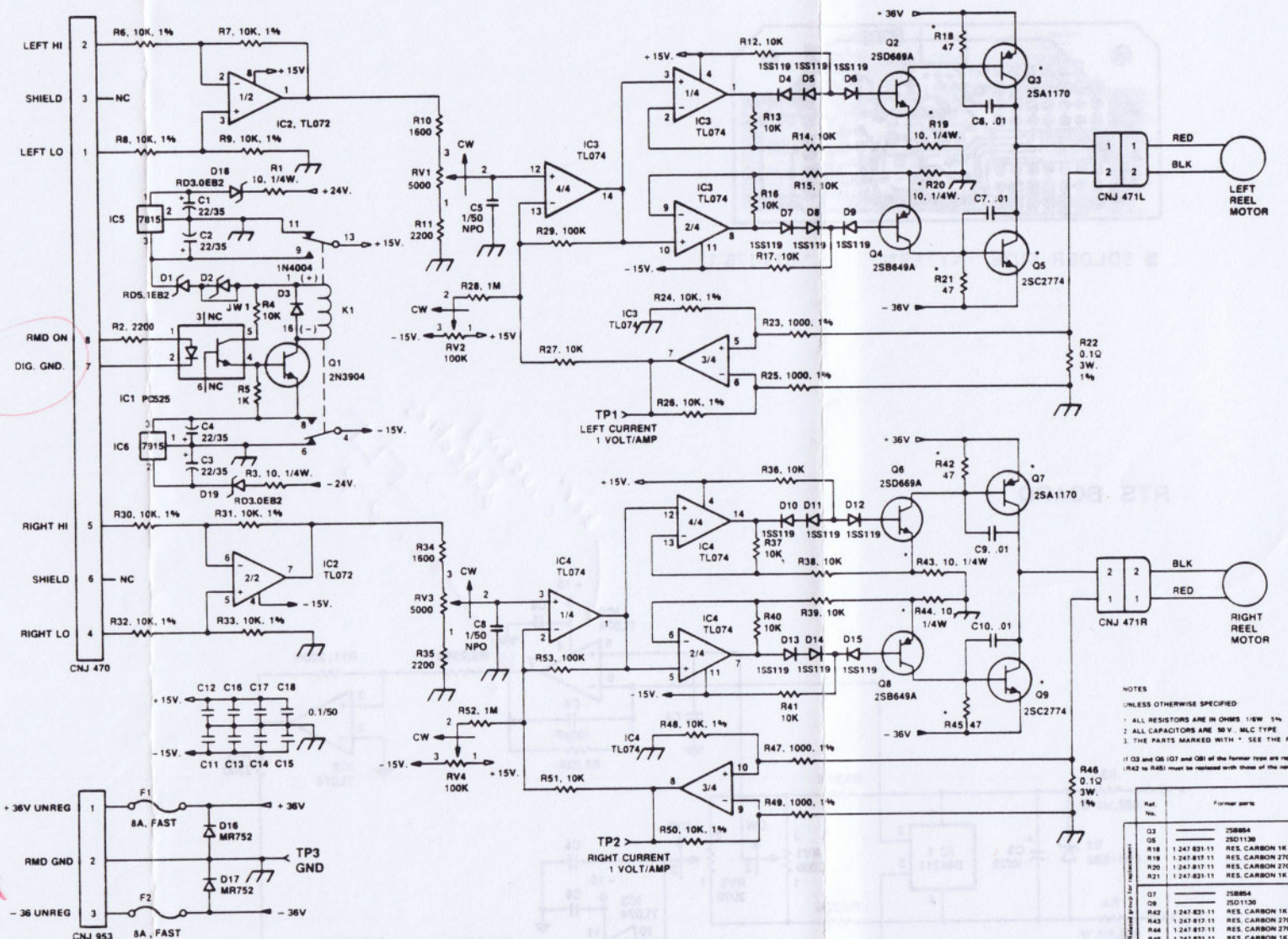


Figure 7-30. MST Board Schematic Diagram (Late Model)

MST BOARD
BOARD NO. 1-619-169-12 & HIGHER
APR-5002/5003V



SOLDER SIDE PATTERN 1-619-160-11



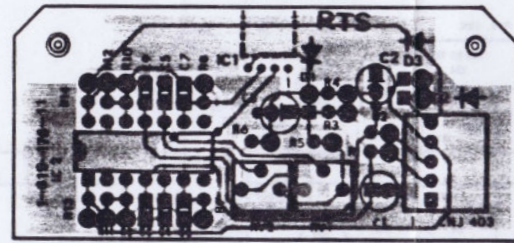
*Pull connector -
tape will
not run
machine
can be
put in wheel -
no tape puller*

NOTES
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS 1%W 5%
2. ALL CAPACITORS ARE 50V. MLC TYPE
3. THE PARTS MARKED WITH * SEE THE FOLLOWING TABLE
* Q2 and Q6 (Q7 and Q8) of the former type are replaced with those of the new type. R18 to R21 (R42 to R48) must be replaced with those of the new type at the same time.

Part No.	Former parts	New parts
Q2	25B854	8 179-300-24 25A1170
Q6	25D1136	8 179-300-18 25C2774
R18	1 247-831-11 RES. CARBON 1K	1 249-493-11 RES. CARBON 47
R19	1 247-817-11 RES. CARBON 270	1 247-688-11 RES. CARBON 18
R20	1 247-817-11 RES. CARBON 270	1 247-688-11 RES. CARBON 18
R21	1 247-831-11 RES. CARBON 1K	1 249-493-11 RES. CARBON 47
Q7	25B854	8 179-300-24 25A1170
Q8	25D1136	8 179-300-18 25C2774
R42	1 247-831-11 RES. CARBON 1K	1 249-493-11 RES. CARBON 47
R43	1 247-817-11 RES. CARBON 270	1 247-688-11 RES. CARBON 18
R44	1 247-817-11 RES. CARBON 270	1 247-688-11 RES. CARBON 18
R45	1 247-831-11 RES. CARBON 1K	1 249-493-11 RES. CARBON 47

Figure 7-31. RMD Board Layout/Schematic Diagram

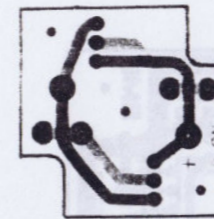
RTS BOARD (1-619-176-11)
Component Side



■ SOLDER SIDE PATTERN 1-619-176-11

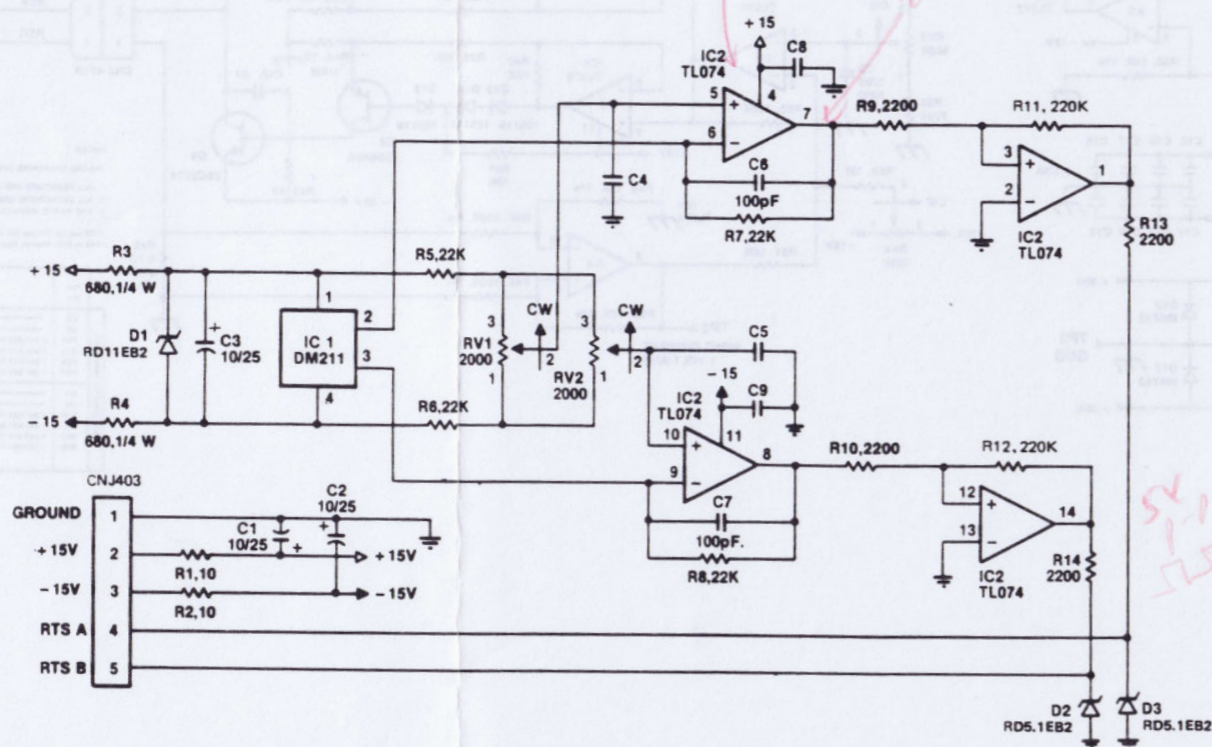
SBR BOARD (1-620-303-11)
Component Side

S/N; APR-5002 20001 TO 20700 ONLY



■ SOLDER SIDE PATTERN 1-620-303-11
■ COMPONENT SIDE PATTERN 1-620-303-11

RTS BOARD



NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ARE IN OHMS, 1/8W, 5%.
2. ALL CAPACITORS ARE 0.1μF, 50 V, CERAMIC.
3. C4, C5 ARE NOT INSTALLED.

SBR BOARD

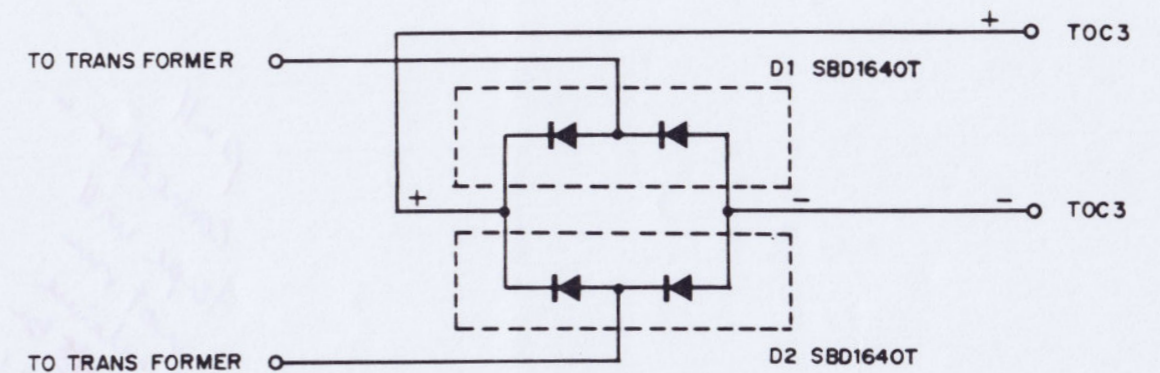


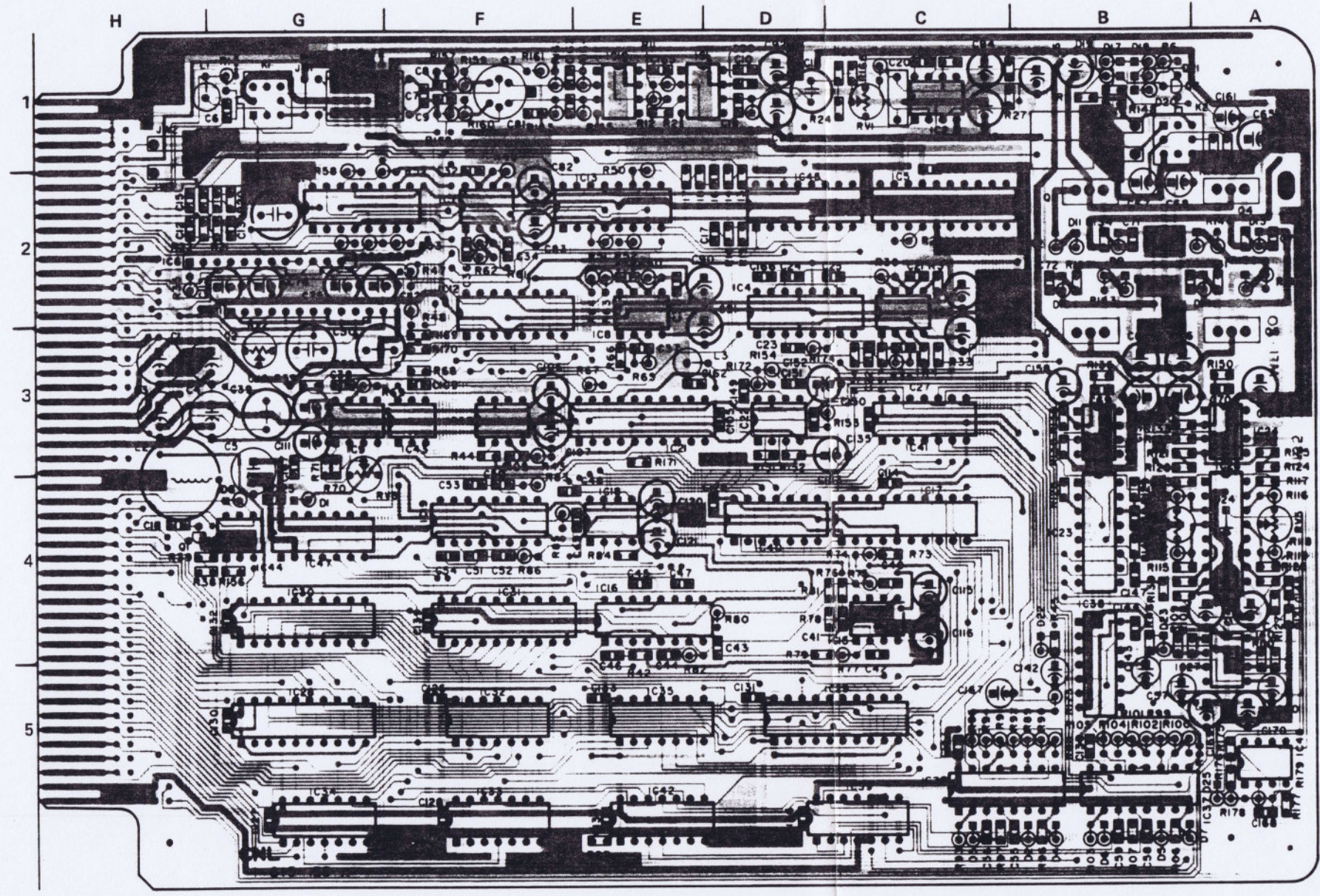
Figure 7-32. RTS Board Layout/Schematic Diagram and SBR Board Layout/Schematic Diagram

RTS BOARD
BOARD NO. 1-619-176-11 & HIGHER
APR-5002/5003V

SBR BOARD
BOARD NO. 1-620-303-11
APR-5002

TCC BOARD (1-619-158-11)
Component Side

S/N: APR-5002 20001 TO 20300



■ SOLDER SIDE PATTERN 1-619-158-11

Figure 7-33. TCC Board Layout (Early)



B SOLDER SIDE PATTERN 1-818-1871

Figure 1-33. TCC Board Layout (Entry)

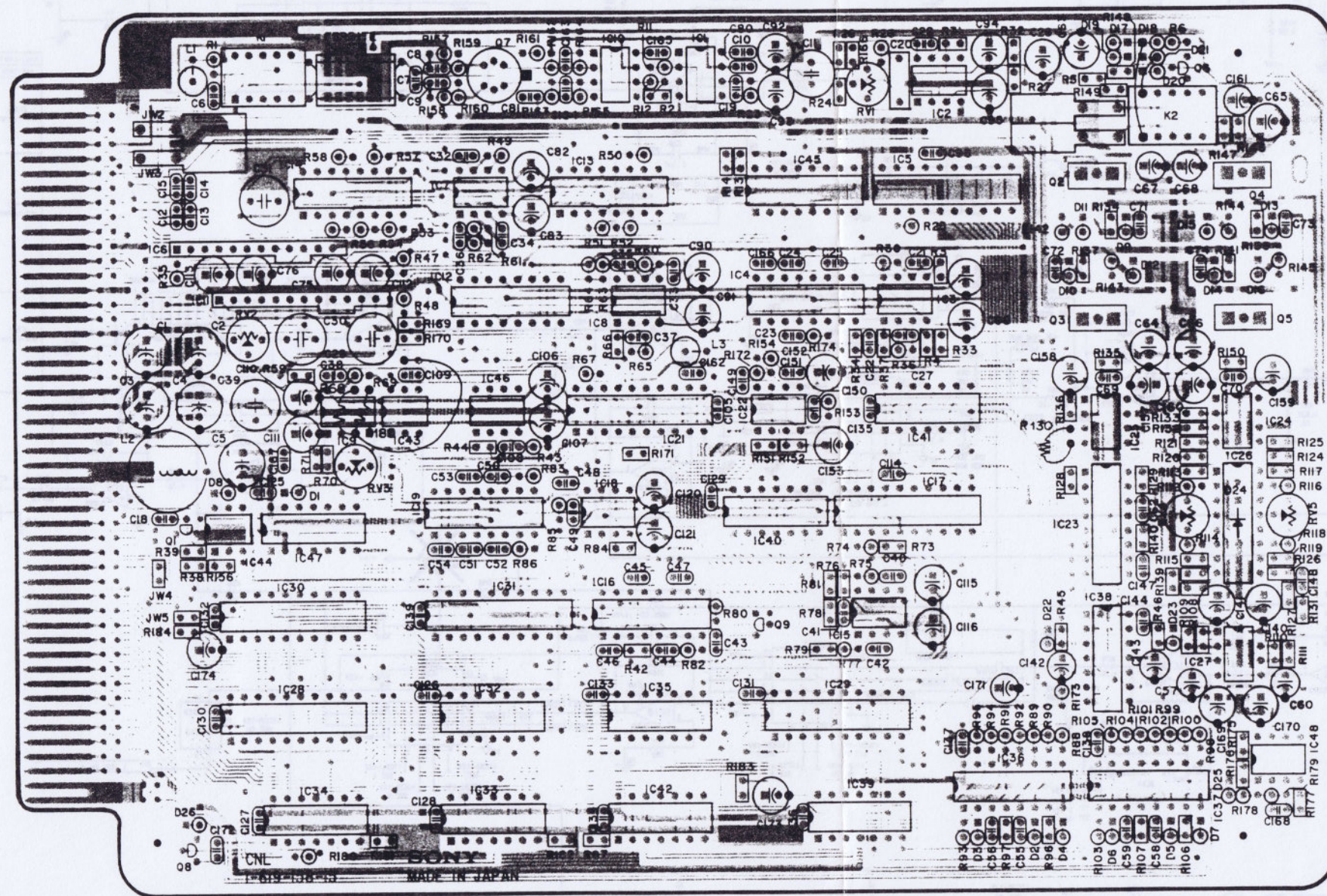
REV APR-2005 50001 TO 50300

TCC BOARD (1-818-188-11)
Component Side

TCC Main Unit

TCC BOARD (1-619-158-15)
Component Side

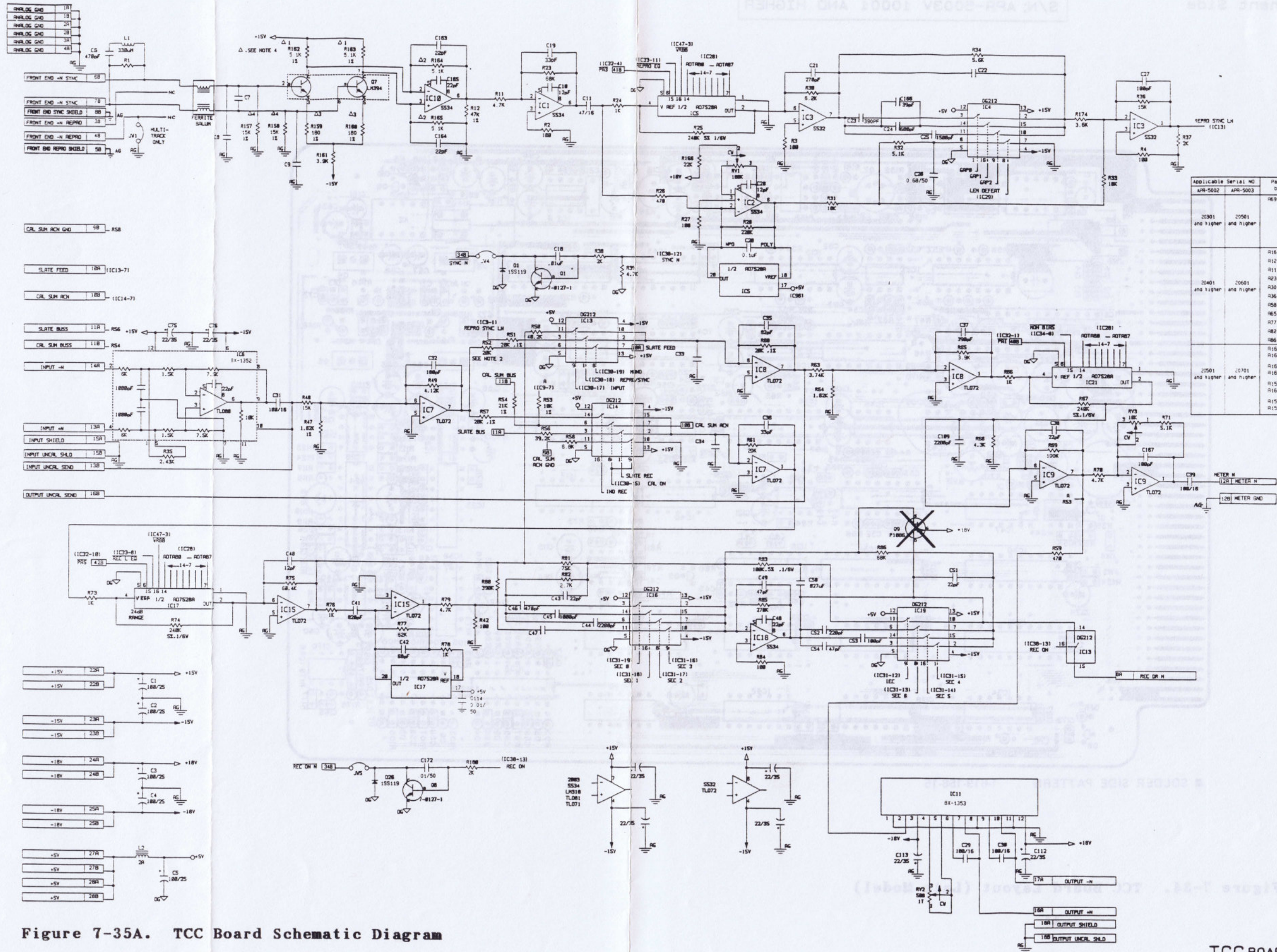
S/N; APR-5002 20301 AND HIGHER
S/N; APR-5003V 10001 AND HIGHER



■ SOLDER SIDE PATTERN 1-619-158-15

Figure 7-34. TCC Board Layout (Late Model)

TCC BOARD



Applicable Serial No APR-5002	APR-5003	Parts that have been changed	Parts that have been added	Parts that have been deleted
20301 and higher	20501 and higher	R69 50 k → 100k	J4 J5 D26 1M914 C172 01/100 DB 7-0127-1 R180 2k	09 P1086
20401 and higher	20601 and higher	R161 3.3k → 3.9k R12 47.5k → 47k R11 4.75k → 4.7k R23 66.5k → 68k R30 6.19k → 6.2k R36 15.4k → 15k R58 6.49k → 6.8k R65 3.83k → 3.9k R77 50.4k → 62k R82 2.7k → 2.7k R86 68.1k → 68k		
20501 and higher	20701 and higher	R162 5.11k → 5.1k R163 5.11k → 5.1k R164 5.11k → 5.1k R159 182 → 180 R158 14k → 15k		

Figure 7-35A. TCC Board Schematic Diagram

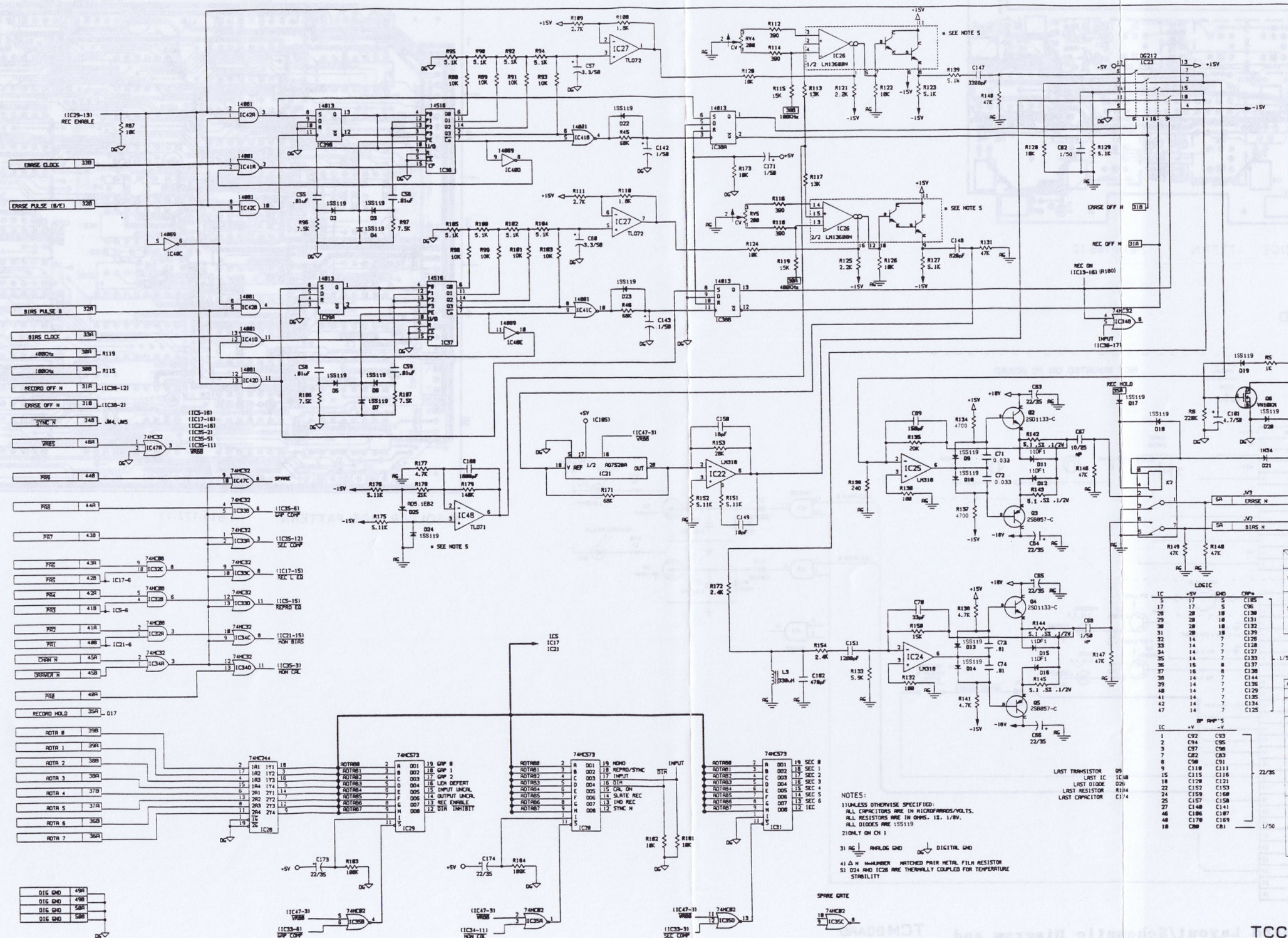


Figure 7-35B. TCC Board Schematic Diagram

FEK DML TCC	1-619-179-11 -12	1-619-179-13 and higher
1-619-158-11 -12	No Problem	Can't use
1-619-158-13 and higher	ADD: J4 Delete: J5	ADD: J5 Delete: J9 and J4

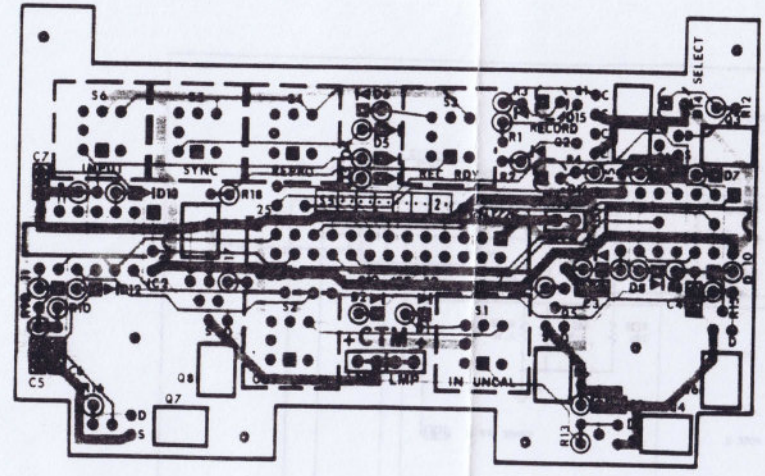
IC	+5V	DND	CFP
17	17	5	C185
17	17	5	C96
28	28	18	C138
28	28	18	C131
36	28	18	C132
31	28	18	C139
32	14	7	C126
33	14	7	C128
34	14	7	C127
35	14	7	C133
36	16	8	C137
37	16	8	C138
38	14	7	C144
39	14	7	C136
48	14	7	C129
41	14	7	C135
42	14	7	C134
47	14	7	C125

Applicable Serial NO	Parts that have been soldered	Parts that have been changed
APR-5002 and higher	APR-5003 and higher	D1 → J4, J5
20301 and higher	20501 and higher	
20401 and higher	20601 and higher	
		R90, R92, R94, R95, R100, R102, R104, R105 5.1K → 5.1K R88, R89, R91, R93, R98, R99, R101, R103 10.2K → 10K R12, R14, R15, R18 402 → 390 R154, R172 2.55K → 2.4K R115, R119 10K → 15K R2, R4 D44C9 → 25D1133-C D45C9 → 25B857-C R11, R2, R5, R8 J8S102 → 110F1

NOTES:
 1) UNLESS OTHERWISE SPECIFIED:
 ALL CAPACITORS ARE IN MICROFARADS/VOLTS.
 ALL RESISTORS ARE IN OHMS, 1% 1/8W.
 ALL DIODES ARE 1SS119
 2) ONLY ON CH 1
 3) AC = ANALOG GND DG = DIGITAL GND
 4) Δ H = HALFWIDTH MATCHED PAIR METAL FILM RESISTOR
 5) D24 AND IC28 ARE THERMALLY COUPLED FOR TEMPERATURE STABILITY

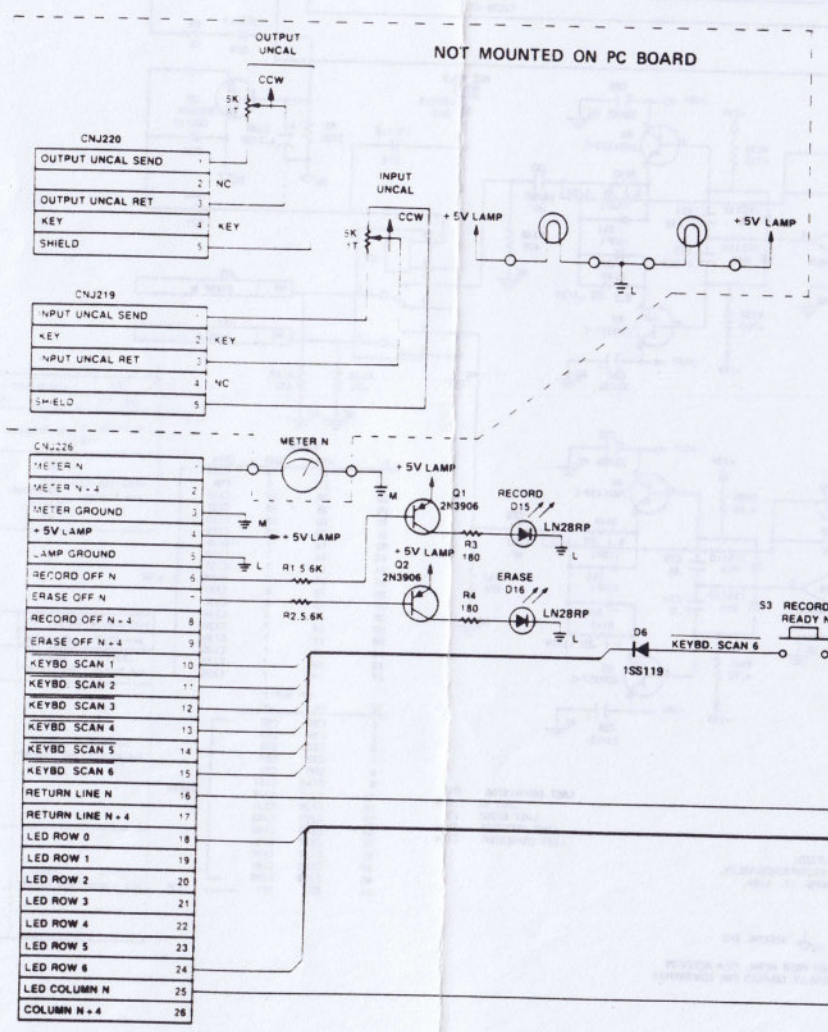
LAST TRANSISTOR Q9
 LAST IC IC18
 LAST DIODE D26
 LAST RESISTOR R104
 LAST CAPACITOR C174

TCM BOARD (1-619-165-12) APR-5003V ONLY
Component Side

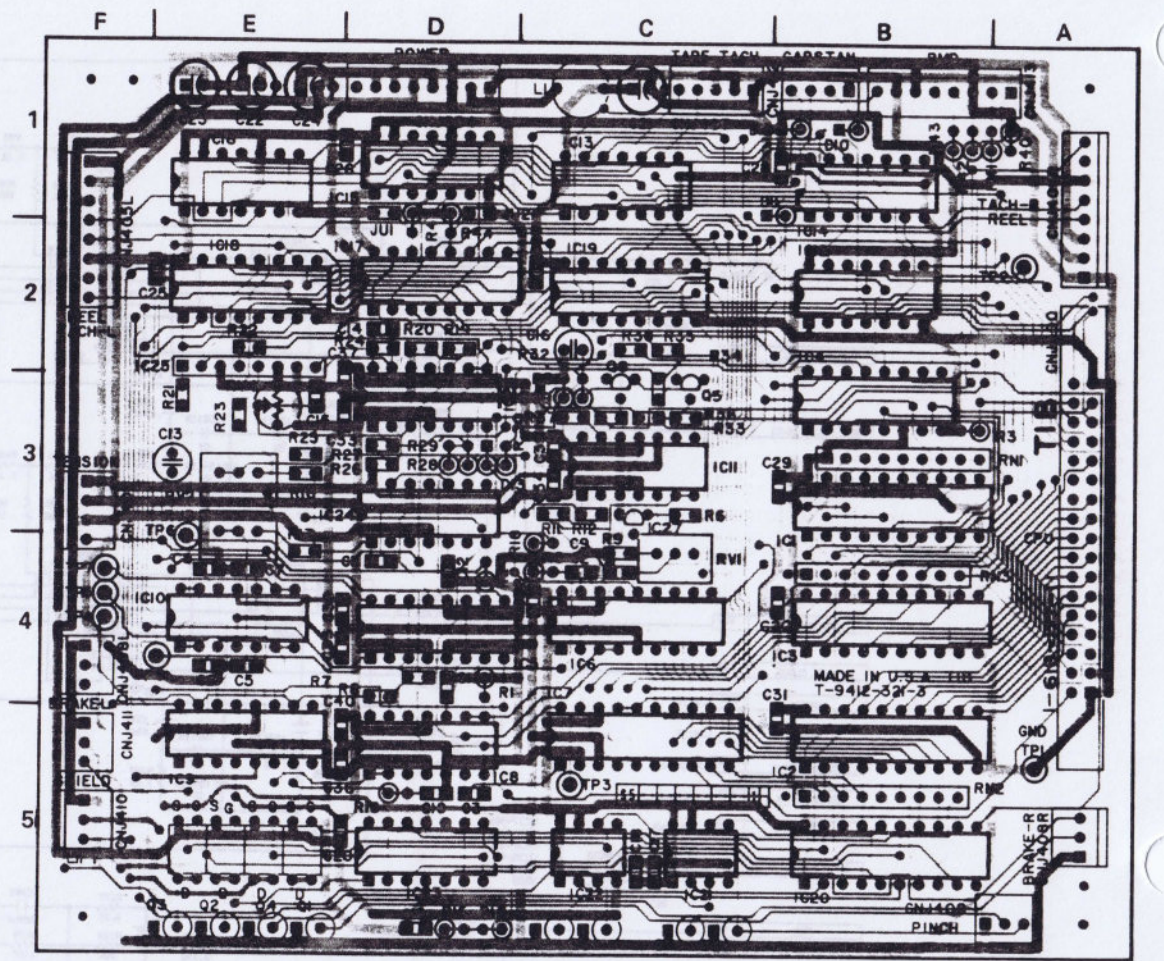


SOLDER SIDE PATTERN 1-619-165-12

TCM BOARD



TIB BOARD (1-619-177-11)
Component Side



SOLDER SIDE PATTERN 1-619-177-11

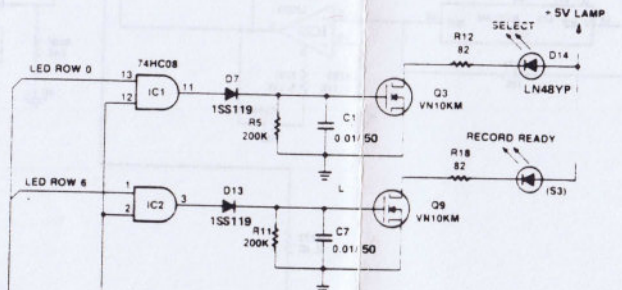
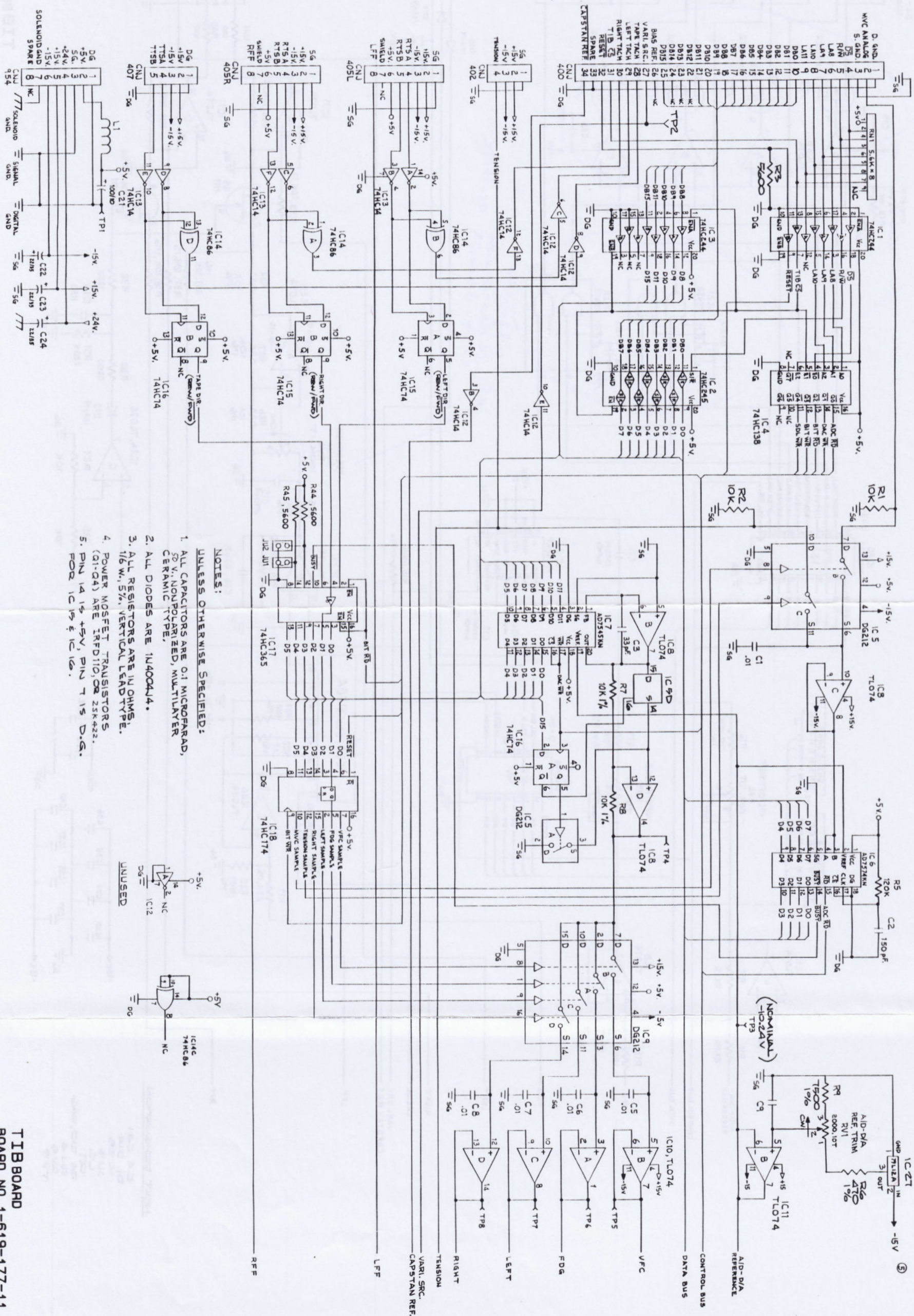


Figure 7-36. TCM Board Layout/Schematic Diagram and TIB Board Layout

TCM BOARD
BOARD NO. 1-619-165-12 & HIGHER
APR-5003V ONLY



- NOTES:
1. ALL CAPACITORS ARE 0.1 MICROFARAD, 50 V., NONPOLARIZED, MULTILAYER CERAMIC TYPE.
 2. ALL DIODES ARE 1N4004/4.
 3. ALL RESISTORS ARE IN OHMS, 1/6 W., 5%, VERTICAL LEAD TYPE.
 4. POWER MOSFET TRANSISTORS (01-04) ARE IRFD110, OR 2SK422.
 5. PIN 14 IS +5V, PIN 7 IS D.G. FOR IC 15 & IC 16.

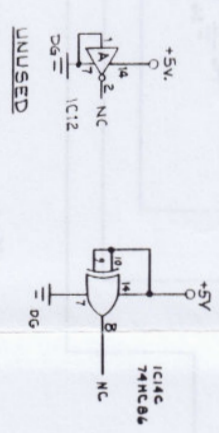
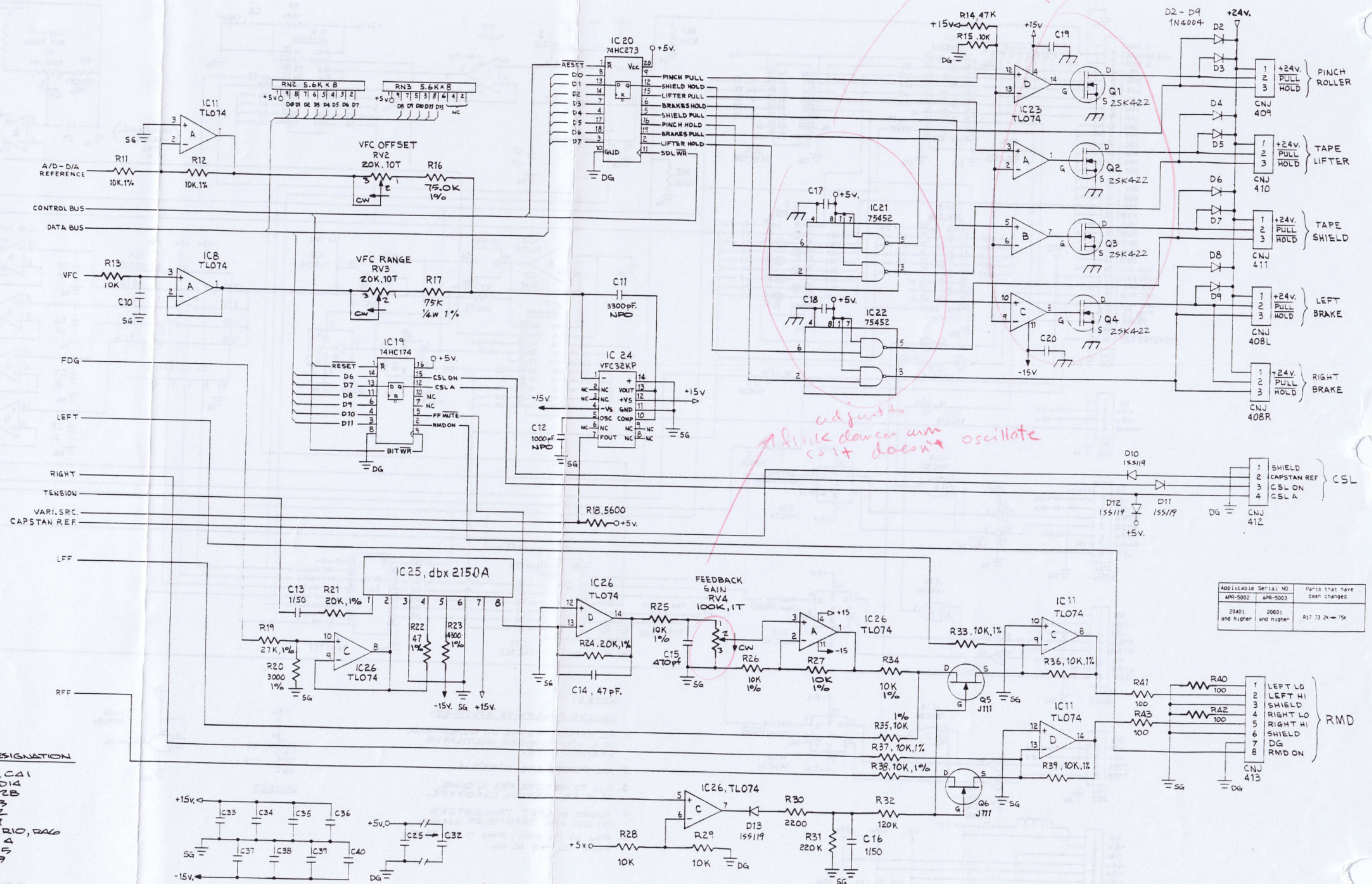


Figure 7-37A. TIB Board Schematic Diagram

TIB BOARD



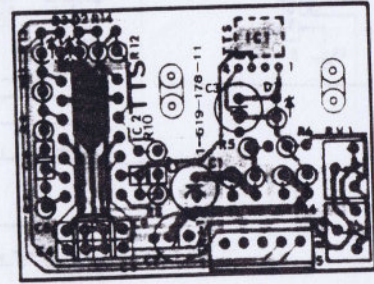
NEXT DESIGNATION
 CA, CA1
 D1, D14
 IC 2B
 JL 3
 L 2
 RA, R7
 RB, R10, R46
 TR 9
 9

Applicable Serial No.	Parts that have been changed
APR-5002 and higher	APR-5003 and higher
20401 and higher	20601 and higher
	R17 75K → 75K

Figure 7-37B. TIB Board Schematic Diagram

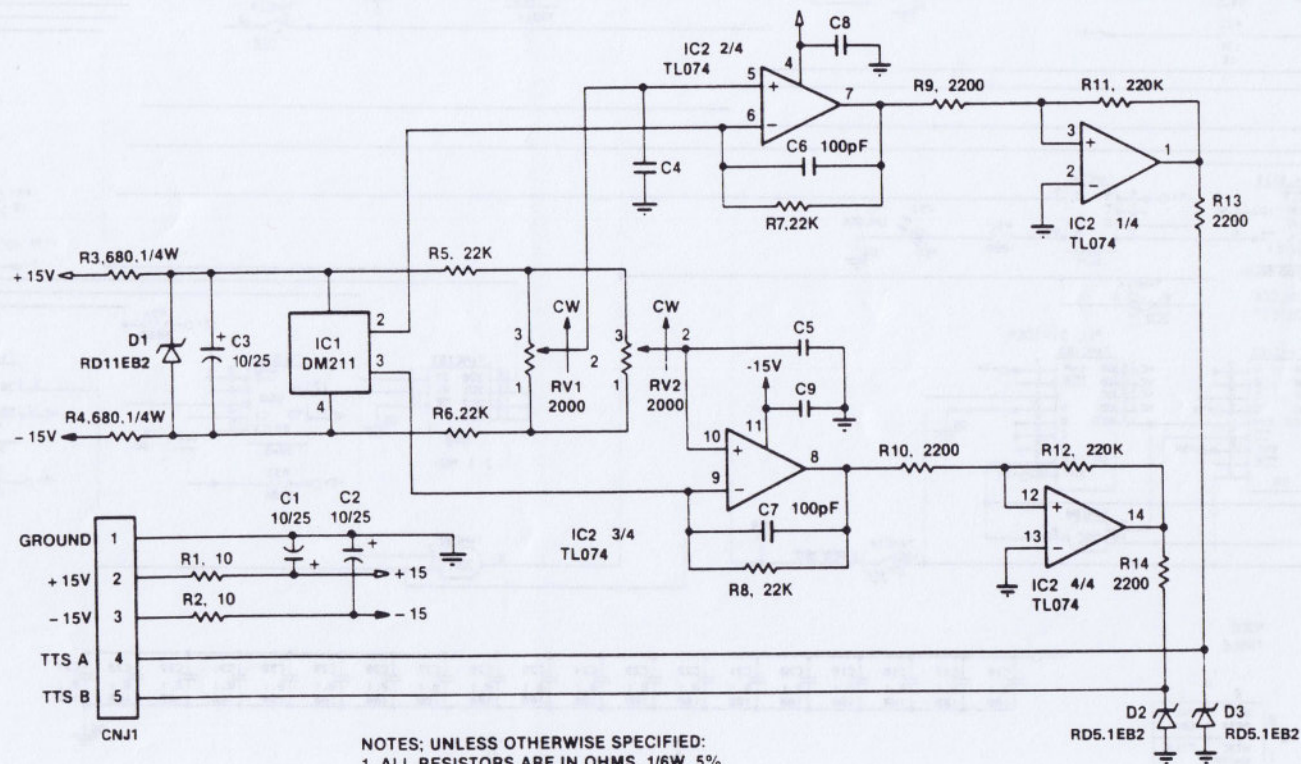
TTS BOARD (1-619-178-11)
Component Side

VVT BOARD (T-9413-749-1) APR-5003V ONLY
Component Side

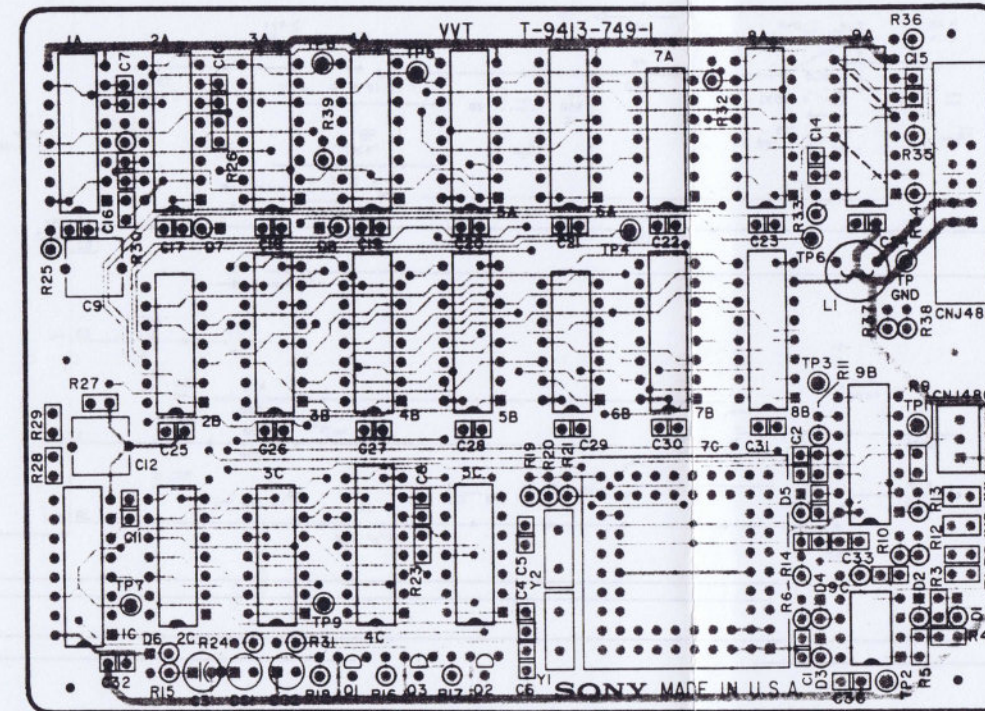


■ SOLDER SIDE PATTERN

TTS BOARD

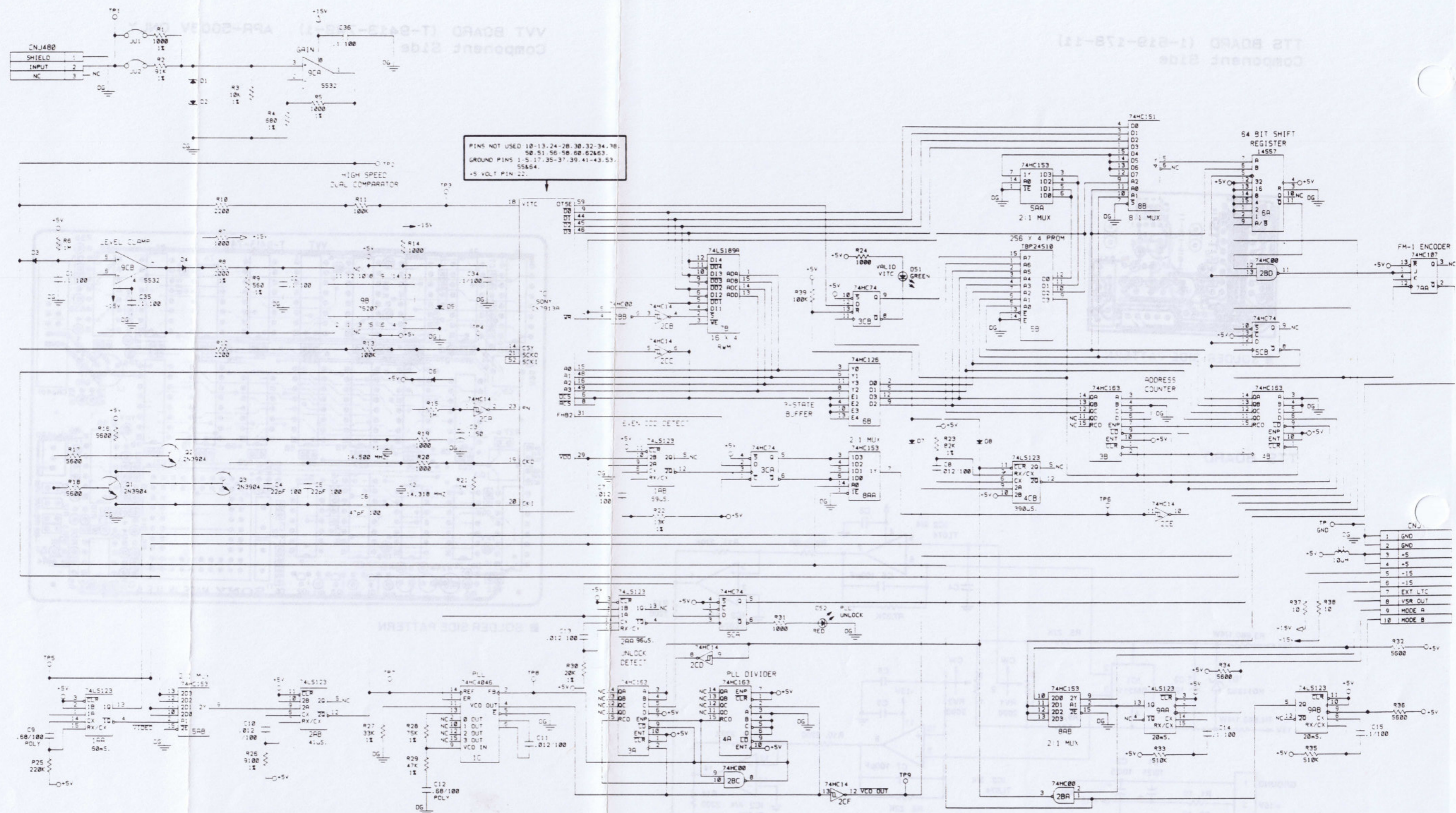


NOTES; UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ARE IN OHMS, 1/6W, 5%.
2. ALL CAPACITORS ARE 0.1μF, 50V, CERAMIC.
3. C4, C5 ARE NOT INSTALLED.



■ SOLDER SIDE PATTERN

Figure 7-38. TTS Board Layout/Schematic Diagram and VVT Board Layout



PINS NOT USED 10-13, 24-28, 30, 32-34, 36, 50, 51, 56-58, 60, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100.

IC	+5V	+5V	GND
1A	C16 .1/100	16	8
2A	C17 .1/100	16	8
3A	C18 .1/100	16	8
4A	C19 .1/100	16	8
5A	C20 .1/100	16	8
6A	C21 .1/100	16	8
7A	C22 .1/100	14	7
8A	C23 .1/100	16	8
9A	C24 .1/100	16	8
2B	C25 .1/100	14	7
3B	C26 .1/100	16	8
4B	C27 .1/100	16	8
5B	C28 .1/100	16	8
6B	C29 .1/100	14	7
7B	C30 .1/100	16	8

IC	+5V	+5V	GND
8B	C31 .1/100	16	8
9B	C33 .1/100	14	7
1C	C32 .1/100	16	8
2C		14	7
3C		14	7
4C		16	8
5C		14	7
7C	C37 .1/100	47.61	40.54
9C			

TEST POINTS
1 INPUT SIGNAL
2 INPUT X GAIN/LOSS
3 LOGIC LEVEL VITC
4 LOGIC LEVEL SYNC
5 VERTICAL DETECT
6 FRAME DETECT
7 PLL REFERENCE
8 PLL FEEDBACK
9 VCO OUTPUT

MODE TABLE	0	1
BY-PASS	0	1
NTSC	0	0
SMPT E	1	0
FILM	0	1

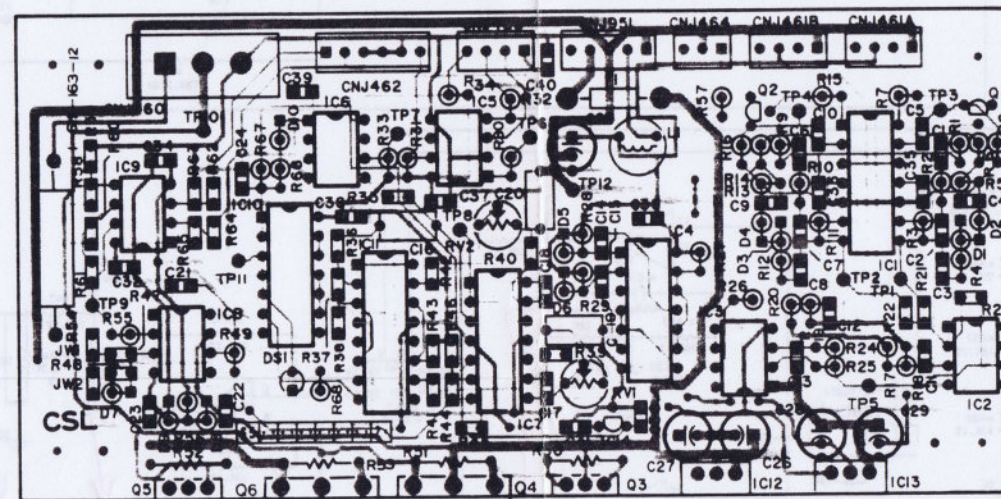
NOTES:
 1) UNLESS OTHERWISE SPECIFIED
 ALL RESISTORS ARE IN OHMS. 5% 1/8W.
 ALL CAPACITORS ARE IN MICROFARADS/VOLTS MLC TYPE
 ALL DIODES ARE 1N914.
 ALL ZENERS ARE 1N5231B.
 ALL 1% RESISTORS ARE RADIAL LEADFORM. 1/8W, METAL.

VVT BOARD
 BOARD NO. T-9413-749-1 & HIGHER
 APR-5003V

Figure 7-39 VVT Board Schematic Diagram

CSL Power Supply

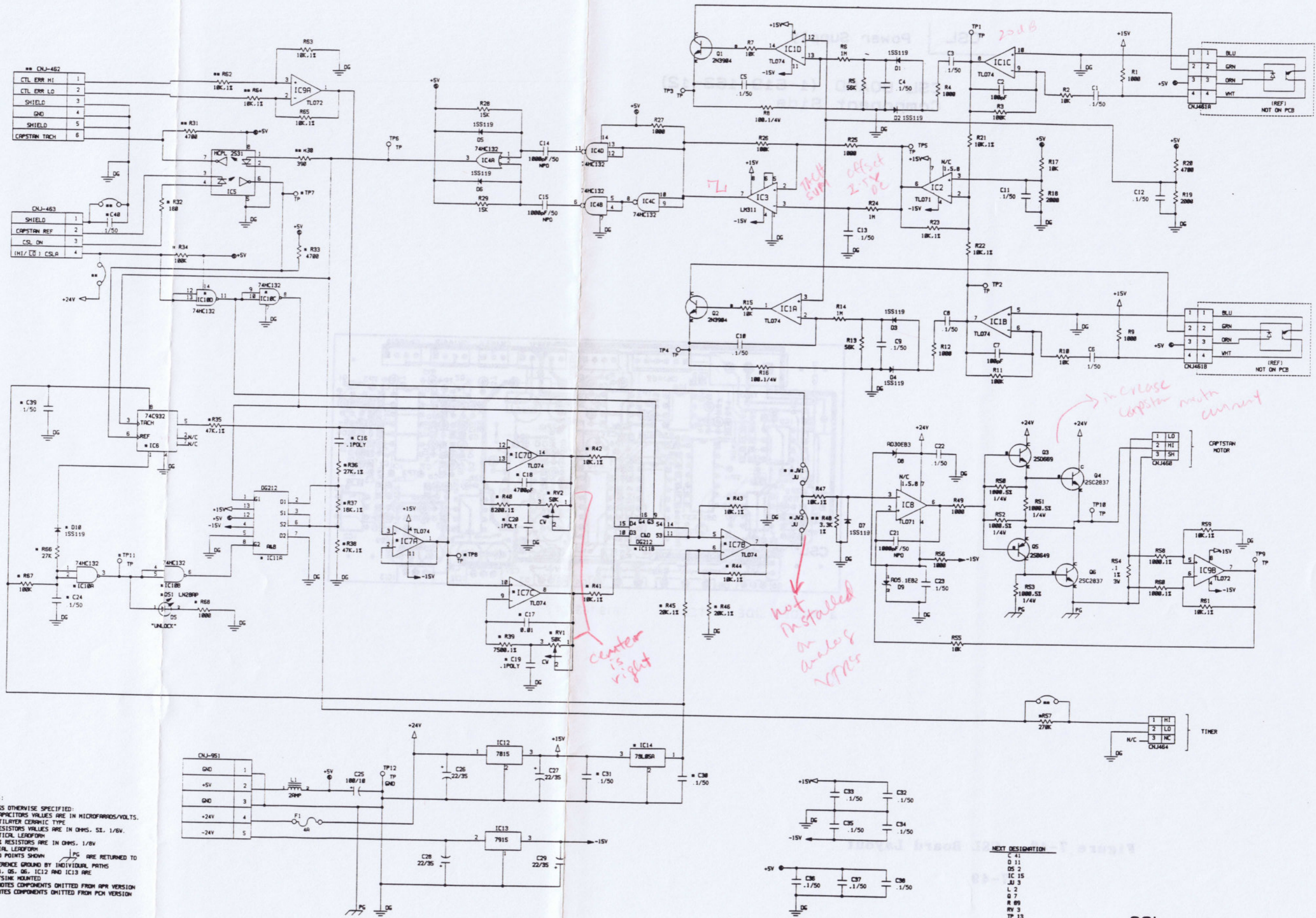
CSL BOARD (1-619-163-12)
Component Side



1 SOLDER SIDE PATTERN 1-619-163-12

Figure 7-40. CSL Board Layout

CSL BOARD

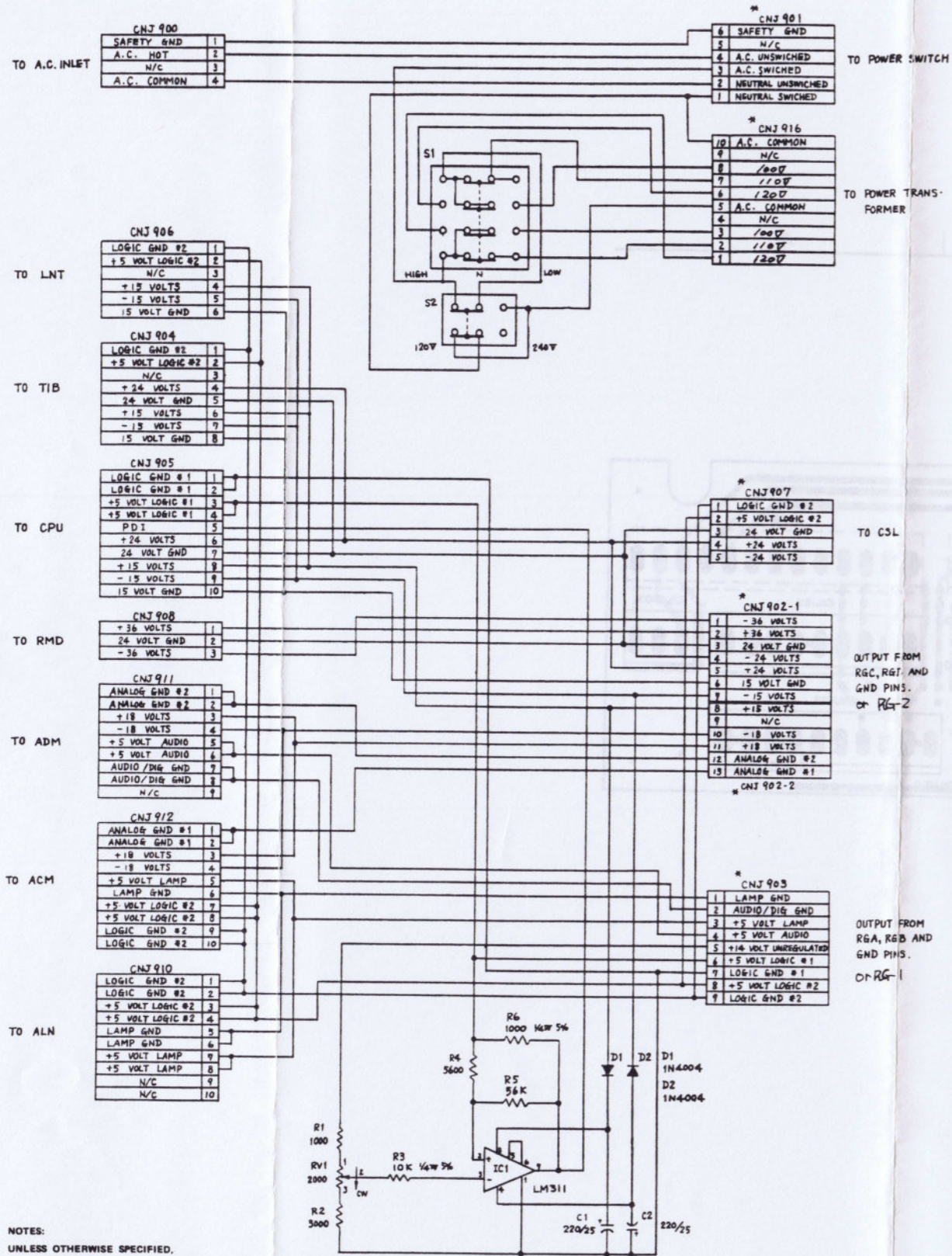


NOTES:
 UNLESS OTHERWISE SPECIFIED:
 1) ALL CAPACITOR VALUES ARE IN MICROFARADS/VOLTS.
 MULTILAYER CERAMIC TYPE
 2) ALL RESISTOR VALUES ARE IN OHMS. SI. 1/6V.
 VERTICAL LEADFORM
 3) ALL 1% RESISTORS ARE IN OHMS. 1/8V
 RADIAL LEADFORM
 4) GROUND POINTS SHOWN ARE RETURNED TO
 REFERENCE GROUND BY INDIVIDUAL PATHS
 5) 03, 04, 05, 06, IC12 AND IC13 ARE
 HEATSHINK MOUNTED
 6) DENOTES COMPONENTS OMITTED FROM APR VERSION
 * DENOTES COMPONENTS OMITTED FROM PCH VERSION

Figure 7-41. CSL Board Schematic Diagram

CSL BOARD
 BOARD NO. 1-619-163-11 & HIGHER
 APR-5002/5003V

PDB BOARD

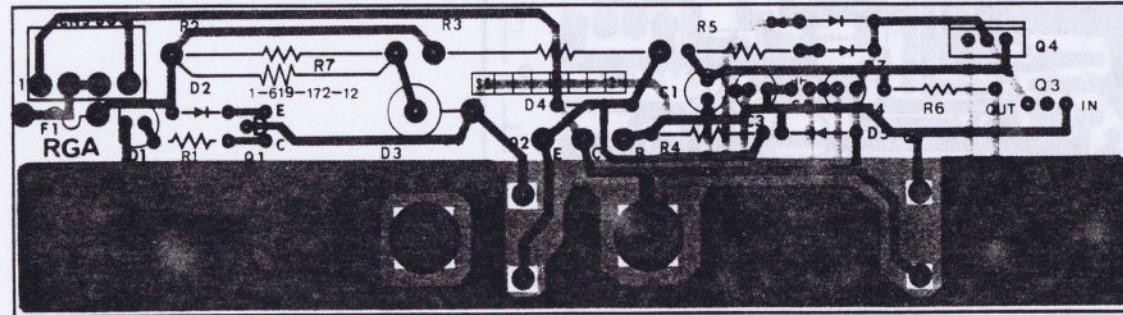


NOTES:
UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTOR VALUES ARE IN OHMS, 1/8W, 1%.
2. CONNECTORS MARKED * ARE LOCATED ON THE SOLDER SIDE OF THE P.C. BOARD.

Figure 7-43. PDB Board Schematic Diagram

RGA BOARD (1-619-172-12)
Component Side

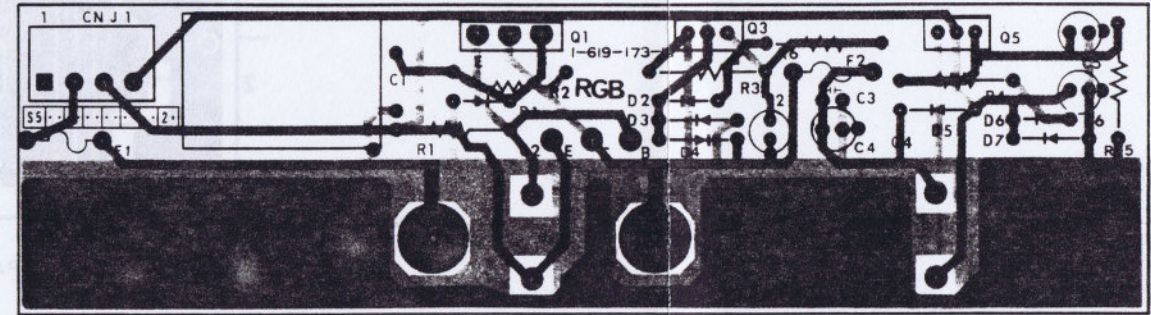
S/N: APR-5002 20001 TO 20615



■ SOLDER SIDE PATTERN 1-619-172-12
■ COMPONENT SIDE PATTERN 1-619-172-12

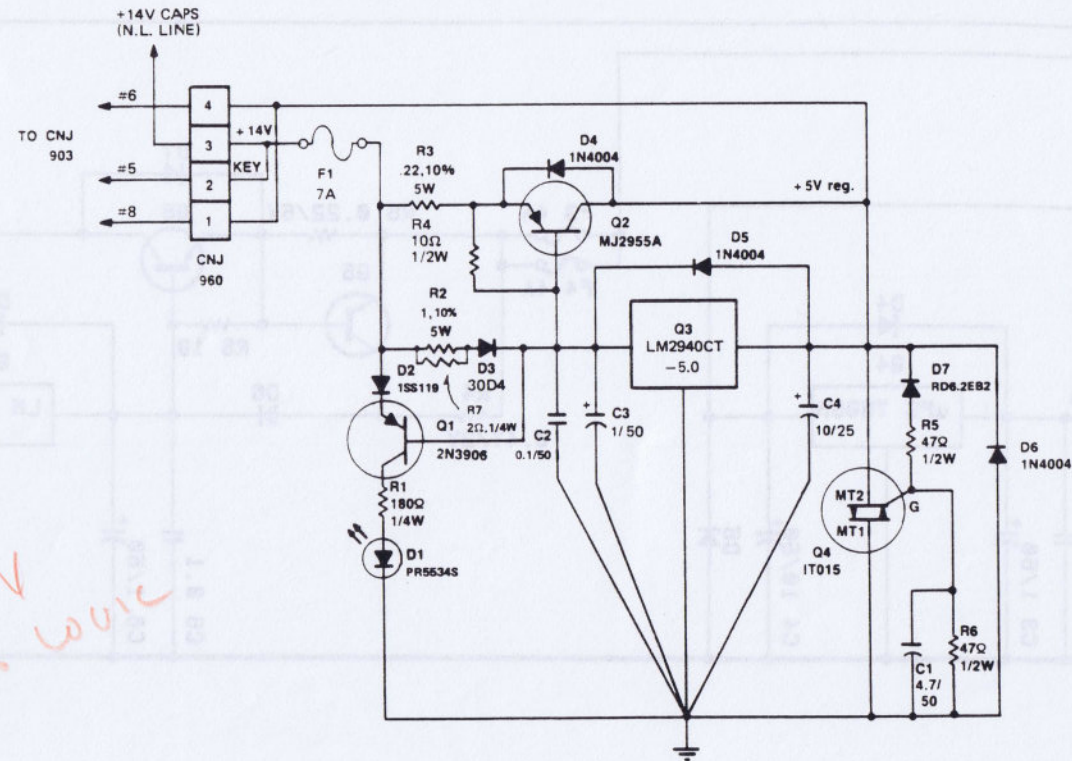
RGB BOARD (1-619-173-12)
Component Side

S/N: APR-5002 20001 TO 20615



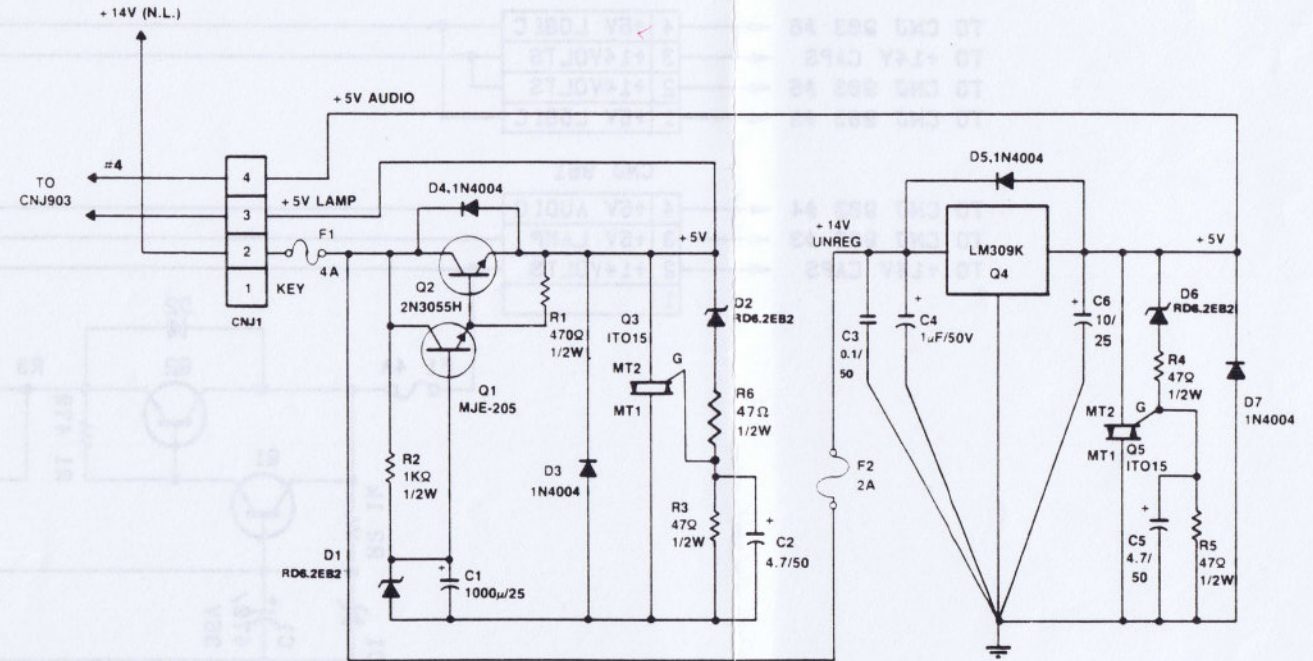
■ SOLDER SIDE PATTERN 1-619-173-12
■ COMPONENT SIDE PATTERN 1-619-173-12

RGA BOARD



*+5V
+ AUDIO*

RGB BOARD



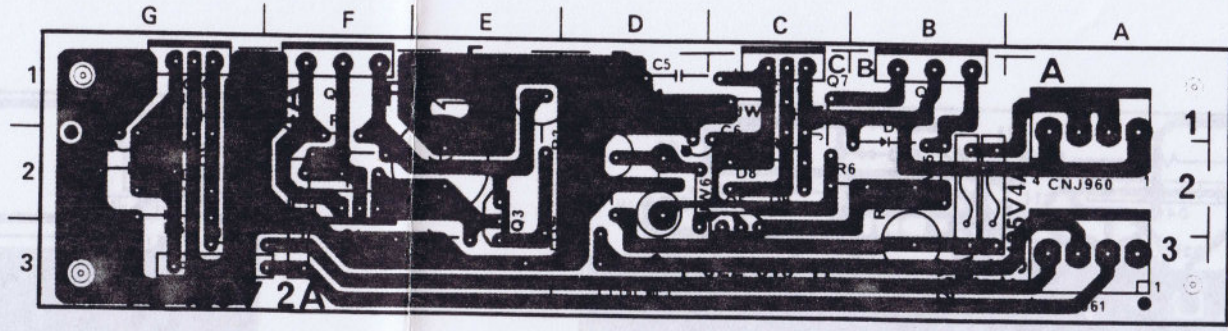
*+5V
AUDIO
LAMPS*

Figure 7-44. RGA and RGB Board Layout/Schematic Diagram

*ALL UNREGULATED VOLTAGE LINES
ARE REFERENCED NO LOAD (N.L.)

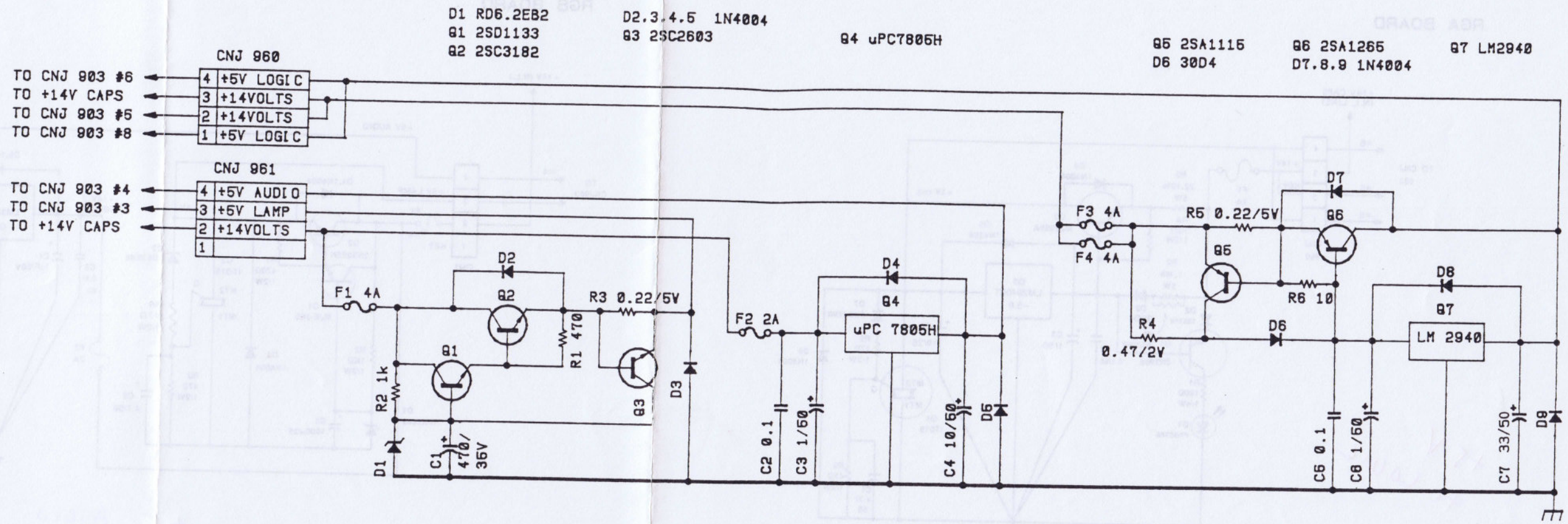
RG-1 BOARD (1-622-916-11)
Component Side

S/N: APR-5002 20701 AND HIGHER
S/N: APR-5003V 10001 AND HIGHER



■ SOLDER SIDE PATTERN 1-622-916-11

RG-1 BOARD



- D1 RD6.2EB2
- B1 2SD1133
- B2 2SC3182
- D2,3,4,5 1N4004
- B3 2SC2603
- B4 uPC7805H
- B5 2SA1115
- D6 30D4
- B6 2SA1265
- D7,8,9 1N4004
- B7 LM2940

Figure 7-45. RG-1 Board Layout/Schematic Diagram

POWER SUPPLY WIRING

S/N; APR-5002 20001 TO 20615

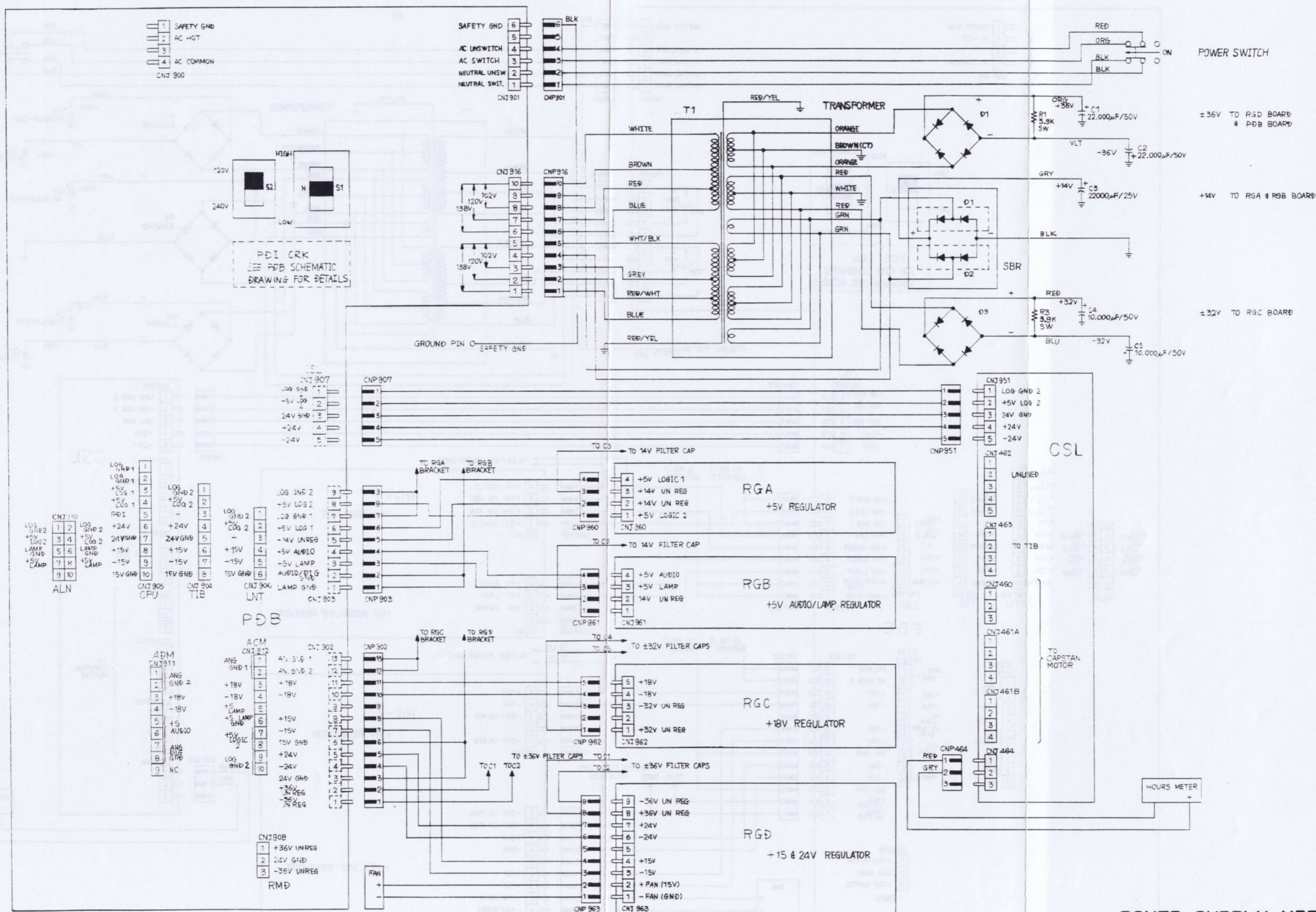


Figure 7-48. Power Supply Wiring Diagram (Early Model)

**SECTION 8
POWER SUPPLY
INFORMATION**

8.0 Overview

The production history of the APR-5000 Series machines encompasses the use of two types of power supply units. For this explanation these power supply units will be referred to as early power supply unit and new power supply unit. The begin/end point for use of each of these power supplies is shown below (as related to machine serial number). The schematic Diagrams for these power supply units can be found in Section 7 of this manual.

Early Power Supply Usage:

APR-5002: Serial # 20001 to 20615

APR-5003: Serial # 20001 to 20825

New Power Supply Usage:

APR-5002: Serial # 20701 and Higher

APR-5003/APR-5003V: Serial # 20901 and Higher

8.1 APR-5000 Series Early Power Supply Unit

The early power supply unit utilizes the four regulator board arrangement. These are the RGA, RGB, RGC, and RGD.

8.1.1 Power Supply Sub-Chassis for Early APR-5000 Units

The Power Supply Sub-Chassis for the early model contains the transformer, rectifiers and filter capacitors for all supply voltages in the APR-5000.

The input voltage (line voltage) is fed to the transformer T1. This is done via the Power Distribution Board (PDB) whereby either 120V or 240V line selection is made and LOW or HIGH line conditions for these voltages can be selected.

The input to the transformer T1 is received via connector CPN916. The output of the transformer is fed to 3 full-wave bridge rectifiers; D1, D2, and D3. Resistors R1, R2, and R3 are used to regulate the variation in the output voltage of the rectifier diodes. Capacitors C1, C2, C3, C4, C5, and C6 provide filtering for the ripple components present.

The output of the sub-chassis are then fed to the inputs of the respective regulator board assemblies.

8.1.3 Regulator Board A (RGA)

Regulator Board A is the +5V regulator for all functions requiring logic level supplies within the APR-5000 transport.

The input to the RGA Board is +14V unregulated no load. This is received via connection CNJ960 on pin 3. The +14VDC is fed into the input of the LM309K or LM2940 through resistor R2 and D3. Capacitors C2 and C3 perform decoupling for both high and low frequencies. Transistor Q2 is used as a pass element to increase the current capabilities of the LM309K or LM2940. Bias voltage is set from the combination of R3 and the network of R2 and D3. The input of the LM309K or LM2940 acts as a base reference for transistor Q2.

Capacitor C4 is used as a filter and to allow slow ramp on of the circuit.

Q1 is part of an indicator circuit showing a short circuit condition of the RGA Board power output (either internal or external to the RGA). Under normal operating conditions the bias of D2 emitter of Q1 to the base of Q1 (R2 and D3) is such that Q1 is turned off, thus no current flow through diode D1.

If an over-voltage condition would exist, the bias of Q1 would change, thus increasing the VBE on Q1 causing LED D1 to light. In addition, the triac Q4 would conduct due to the change in bias on the gate and its network of D7, R5 and R6.

If an external short to ground would exist, the LM309K or LM2940 would exhibit its own internal thermal limiting and diode D would light through the conduction of Q1 being turned on. If a short was present on the output less the ground (negative voltage), D6 would conduct and the crowbar circuit of Q4 would activate. Diodes D4 and D5 around their respective devices create a reverse voltage protection.

In addition, the RGA board feeds +14V to the Power Distribution Board (PDB) which is used by the power down imminent circuit (PDI signal).

The fuse for the +5V power supply is also mounted on this PC board.

8.1.4 Regulator Board B (RGB)

Regulator Board B is the +5V regulator for all audio system and lamp power requirements within the APR-5000 Audio System. Please note that there are two individual power regulator circuits on this board.

The input to the RGB Board is +14VDC unregulated. This is received via pin 2 of connector CNJ961. There are 2 regulators located on the RGB Board. The Lamp and Indicator LED voltage regulator is a discrete design using solid state devices and the +5V Audio System voltage regulator is a 3-terminal monolithic type.

The Lamp Regulator is a series type regulator. Transistor Q1 is the driver element. This device receives the bias voltage from the network of R1, R2, and D1.

As the load increases, the bias voltage on Q1 increases, thus increasing the drive to pass element Q2. If an over-voltage condition would occur, the triac Q3 will conduct. This is caused by changing the bias on the gate of Q3. This threshold is set by the combination of D2, R3, and R6. In the over-voltage condition, Q3 conducts. This provides a reverse bias on D1 causing the conduction of Q1 to decrease or stop.

Capacitors C1 and C2 are for high and low frequency decoupling. If a short circuit on the output is less than ground (negative voltage) this will cause diode D3 and D4 to conduct, thus protecting the regulator circuitry.

The +5V audio uses a standard 3-terminal voltage regulator (LM309K). The input to the regulator is received from pin 2 of CNJ961. Capacitors C3 and C4 provide low and high frequency, decoupling to the input of the regulator. Capacitor C6 provides filtering and slow ramp up of output.

The circuit of Q5, D6, R4, and R5 provide the crowbar protection similar to the +5V lamp supply. Diodes D5 and D7 provide the reverse voltage protection (same as D3 and D4 of the +5V lamp supply).

In addition, fuses for the two power supply rails are provided on-board.

8.1.5 Regulator Board C (RGC)

The +/-18V voltage regulator board consists of two 3-terminal adjustable monolithic type voltage regulators. The adjustment of these regulators are fixed by design, thus no alignment is required.

The input to the negative regulators -32V is received via pin 3 of CNJ962. This is fed to the input of the LM337K. Capacitors C1 and C2 provide decoupling for low and high frequencies. The LM337K acts as a driver/reference for the pass element Q3. Q3 is used as a current amplifier to provide the additional drive capabilities required.

Bias for Q3 is provided by the network of R2, R3, R4, and D3. The output adjustment of the LM337K is set by R16 and R15. D15 provides an alternative path for current in the event of the ground point becoming more positive than ground. Capacitor C3 provides output filtering and slow ramp on time of the 18 volt output.

Q1 is part of an indicator circuit showing a short circuit condition within the RGC Board. Under normal operating conditions, the base of D2 emitter of Q1 to the base of Q1 (R3 and D3) is such that Q1 is turned off, thus no current flow through D1.

If an over-voltage condition would exist, the bias of Q1 would change thus increasing the VBE potential on Q1 causing the indicator LED D1 to illuminate. In addition, the triac Q4 would conduct due to the change in bias on the Gate and its network of D6, R5, and R6.

If an external short to ground would exist, the LM337K would exhibit its own internal thermal limiting and diode D1 would light through the conduction of Q1 being turned on. If a short was present on the output less than ground (negative voltage) D5 would conduct and the crowbar circuit of Q4 would activate. Diodes D4 and D7 around their respective devices create a reverse voltage protection. The +18V regulator uses an LM317K as the driver/reference and employs the same basic circuitry.

Fuses for each of the power supply rails are located on-board.

8.1.6 Regulator Board D (RGD)

Regulator Board "D" is the +/-15V volt and +/-24V Regulators for transport and audio functions in the APR-5000.

The +/-15V is used for the amplifiers throughout the transport system. The +/-24V is used on the Transport Interface Board (TIB) and the Reel Motor Driver Board (RMD). On both the TIB and RMD the +24V supply is regulated to +15V with on-board regulation. The +24V is also used to drive the fan located within the supply. The inputs to the RGD Board are +/-36 volts unregulated no load. These are received via pins 8 and 9 respectively of connector CNJ963.

The +24V regulators are series type as in the +5V lamp supply. The +15V regulators are the 3 terminal monolithic type.

The unique difference in the regulator assembly is that the output of the series regulator (24V) is fed directly to the input of the 3-terminal regulators (15V). Thus, in the event of reverse voltage or overvoltage, the series fed supply will be lost.

A fuse is also incorporated for the power supply rail and this is mounted on the PC board.

8.2 New Power Supply Unit

The TPS unit which contains the RG-1 and RG-2 regulator boards is the new model.

8.2.1 Power Distribution Board

The Power Distribution Board (PDB) is the interconnect between the power supply and the transport and audio electronics. The PDB also incorporates the PDI sensing circuit (IC1). This circuit monitors the +5V (Logic 1) line in a comparator fashion. When power is disconnected from the APR unit, the filter capacitors on the +5V (Logic 1) line will begin to discharge. Once the +5V (Logic 1) line level decreases to the threshold value of the comparator (set by RV1), the comparator output issues the Power Down Imminent (PDI) command to the CPU board. This allows the CPU time to carry-out a smooth power off sequence.

8.2.2 Regulator-1 (RG-1) Board

The Regulator-1 board has been developed to replace the RG-A and RG-B boards. This design change is effective on all APR-5002 and APR-5003/5003V machines as shown below:

- APR-5002: Serial # 20701 and Higher
- APR-5003: Serial # 20901 and Higher

The RG-1 board supplies the following voltages to the APR unit:

- +5V (Logic 1)
- +5V (Logic 2)
- +5V (Audio)
- +5V (Lamp)

8.2.3 Regulator-2 (RG-2) Board

The Regulator-2 board has been developed to replace the RG-C and RG-D boards. This design change is effective on all APR-5002 and APR-5003/5003V machines as shown below:

- APR-5002: Serial # 20701 and Higher
- APR-5003: Serial # 20901 and Higher

The RG-2 board supplies the following voltages to the APR unit:

- +15V
- 15V
- +18V
- 18V
- +24V
- 24V

APPENDIX A

GLOSSARY OF TERMS

- A-B Listening A listening comparison between two audio programs or between two different tracks on the multi-track tape, usually accomplished by switching between the two sources whose signal levels are matched.
- A/D Analog-to-Digital conversion.
- A/D Converter Analog-to-Digital Converter. This device is provided with an analog signal input and produces a digital output which describes the analog input voltage level at that instant in time. When conversions are taken sequentially at equal intervals of time, a sampling of a dynamic signal (such as audio) may be achieved (much as a film camera takes a series of individual photographs and produces a motion picture). The input to an A/D converter stage is normally a sample and hold circuit.
- ACN Active Combining Network. A summing amplifier used to combine multiple signal inputs into a single composite signal line.
- ACM In an APR-5000 Series recorder, the acronym for the Audio Control Motherboard.
- ADM In an APR-5000 Series recorder, the acronym for the Audio Distribution Motherboard.
- AHB In an APR-5000 or an APR-24 Series recorder, the acronym for the Audio Headstack Board.
- ALN In an APR-5000 Series recorder, the acronym for the Audio Alignment Panel Board.
- Active Device Implies the capability of supplying power or voltage gain. All active devices require a power supply.

Alias Frequency This the effect of sampling a frequency which is greater than the Nyquist frequency. It can be calculated by subtracting the input frequency from the Nyquist Frequency.

Alignment The adjustment of a device made in order to conform to published specifications.

Amplifier A circuit which takes an input signal and produces an output which has more power, voltage, or current.

Analog The description of a waveform from whose voltage and frequency varies infinitely over time and whose amplitude is also continuously variable within a certain range.

Anechoic Chamber A room which has no acoustic reflections, also called a "dead" chamber.

Aperture Error This is the difference between the voltage on the input of the sample-and-hold at the time that the sample clock arrives and the actual voltage held by the s/h.

Aperture Time This is the time between the arrival of the sampling clock to the sample-and-hold circuit to when the voltage at the s/h input is held.

Assign A method of routing audio signals to a specific signal path. Usually, this is done by way of a switch which indicates the signal path which will be activated.

Asynchronous A description of a signal that is not synchronized with respect to another signal (usually a reference or house sync signal). Directly, this is the property of being without synchronization.

Attack Time The parameter which determines an audio signal processor's ability to react to sudden bursts of high level program material. Attack describes the beginning of a note or the first portion of the note's envelope in which the note rises from silence to full level.

Attenuation Pad A resistive network used to reduce the level of an audio signal.

Auto-Locator The MCI/SONY tape transport remote controller.

Audio Pertaining to frequencies corresponding to a normally audible sound wave. These frequencies range from approximately 15Hz to 20,000Hz.

Back Porch In a video signal, this is the area of the synchronizing signal immediately following the negative-going sync pulse and preceding the color burst. In the case of a bad edit phasing or bad sync timing, the back porch area may be lost causing color or locking problems.

Back-timing A technique which is used for determining the duration of music used for a background. This is done so that the music ends simultaneously with the narration.

Baffle Any partition designed to obstruct sound waves providing acoustic isolation. Also called a gobo or splay.

Balance The relative levels between two audio sources. The stereo balance generally implies the left and right signal level comparison. A BALANCE control circuit has two inputs and two outputs, never introducing signals from one circuit to the other. A common example is the BALANCE control found on the typical consumer stereo product. Moving the control causes one channel to be attenuated and the other to be amplified, but at no point does the right channel signal pass to the left channel output.

Balanced A differential output or input is said to be balanced because there is signal on both of the signal lines (hot and cold). The signal lines are at equal potential but opposite polarity with respect to ground.

Bandpass Filter A filter that attenuates above and below a desired range of frequencies (bandwidth).

Basic Tracks In multi-track recording, those tracks which are recorded first. This is usually the rhythm tracks.

Bass Trap A baffle which is more effective for absorbing the low frequency sound waves.

Bi-Amplification A monitoring system in which the woofer and tweeter are driven from separate power amplifiers. Generally, an active crossover is used to separate the low and high frequencies for each of the amplifiers.

Binary Resistive Ladder A type of D/A converter whereby each bit of the digital data activates a switch which is part of a resistor ladder so that each switch will add twice as much current as the previous switch. The sum of all of the switches is the analog output.

Blanking In a video signal, blanking pulses are part of the complete synchronizing signal. It is used by TV cameras and monitors to turn off the beam as it retraces to start another line of the camera or screen.

Bouncing Tracks The process of mixing tracks on a multi-track tape and recording them on an unused track. Also called Dump operation.

Buffer An intermediate isolation stage between a signal source and its destination. The buffer presents a constant load to the source, and reduces the source impedance to the next stage.

Burn-In The process of leaving electronic equipment with power turned ON for an extended period of time. This is done because most electronic components have been found to fail within the first 72 hours of continuous operation.

Burst Flag This is a pulse, found on the output of most video sync generators, which is used by other video equipment to control the timing of the color burst on the back porch of each horizontal sync pulse.

Bus A group of lines or conductors used to carry multiple electrical signals. Usually, these are shown as a thick line in a schematic diagram, however this does imply a series of individual traces or conductors. This word is very often misspelled as "buss".

CNL In an APR-5000 Series recorder, the acronym for the Audio Channel PC Card.

CNX In an APR-5000 Series recorder, the acronym for the Connector Interface Board.

CNX-II In an APR-5000 Series recorder (post APR-5003V model release), the acronym for the revised Connector Interface Board.

CPU In an APR-5000 Series recorder, the acronym for the Central Processing Unit Board.

CSL In an APR-5000 or an APR-24 Series recorder, the acronym for the Capstan Servo Loop Board.

CTM In an APR-5000 Series recorder, the acronym for the VU Meter Controller Board.

Channel A group of circuits and controls associated with the I/O Module used to feed an audio signal to a track of the Multi-track recorder.

Channel Bus A summing bus which carries all of the signals to be fed to the Multi-track.

Channel Circuit In a console, this describes the group of circuits and controls used to feed audio signals to the multi-track tape recorder.

Clean A signal which is free of noise, distortion, special effects, equalization, clipping, and leakage.

Clear A signal which is free of noise, distortion, clipping, and leakage. It can be heard distinctly in the mix, easily differentiated from the other sounds. Not "dull" or "muddy".

Coherence A measure of the interrelationship between the synchronization pulses and the sub-carrier (color) components of a video signal.

Color Bars A universal video test signal which contains all of the saturated primary and secondary colors (also gray and white).

Color Burst The color information area of a video signal located on the back porch of every horizontal sync pulse.

Comm Function A talkback function which allows the console operator to speak over the cue buses without disrupting the signals going to tape.

Comm Module Communication module. This module provides communication facilities between the console operator and the studio. The module also contains Slate and Test oscillators.

Complex Waveform A waveform which has more than one frequency component.

Composite Digital This is a pseudo-video signal which contains the multiplexed HDM-1 encoded digital audio data (includes error correction codes, interleaving, and synchronization characters) and the blanking and synchronization signals. This is very similar to monochrome composite video signals.

Composite Video This describes the complete video signal including the picture signal and the blanking and synchronization signals. For color, color information is also added to the signal.

Compression Ratio In a compressor, this describes the amount of level change of the input signal required to change the output signal level by 1dB.

Control Room The room in which the engineer controls and monitors the recording or mix-down session. This would also be the location of the mixing console.

Convection-Cooled The transfer of heat by means of mass movement of hot air particles.

Crossover An electronic network used to divide the incoming signal into two or more frequency bands.

Crosstalk Generally this occurs between two adjacent signal lines where the signal from one line is detected in the other. Most often this is caused by proximity of the wiring or improper shielding techniques.

Cue A monitor system that allows musicians to hear themselves and the previously recorded tracks, usually the headphone source. Sometimes called Foldback.

DSP 1) In an APR-5000 Series recorder, the acronym for the Display Board. 2) When referring to a digital audio system, Digital Signal Processing

D/A Converter Digital-to-Analog Converter. This is used to convert digital data to an analog voltage.

Dead A room, recording, or microphone placement which has little or no reverberation.

Decay The portion of a note or envelope in which the signal deteriorates from full level to a low or mid-range level. The decay time or reverberation time, also called RT60, is the time it takes the reverberator output to fall 60dB below the steady state level.

Decibel A logarithmic ratio used to express a power or voltage level in relation to some given reference.

De-Emphasis This is the emphasis signal conditioning process used on the D/A converter circuitry. It provides a high frequency attenuation on the same order as the boost provided by the pre-emphasis circuit.

De-esser A signal processor used to remove excessive sibilance by compressing the high frequencies around 5 to 10kHz.

Delta Modulation A method of reducing the error and increasing the precision of a PCM system. It involves feeding a 1-bit correction signal back to the input of the system.

Depth The audible sense of closeness or distance of various instruments. Those with little or no reverberation are generally perceived as being close, those with more reverberation are generally perceived as being far.

Differential Line Input A balanced audio input. This input measures the difference between two signal line inputs (as from a differential line output). The advantage of the differential input stage is the fact that when in-phase signals are presented to the two input signal lines, such as noise induced into the audio cabling, the DIS will "reject" these signals as there will be no difference between the two inputs. This ability is measured as the common mode rejection ratio.

Differential Line Output A balanced audio output. This provides two output signal lines, and commonly a ground reference used for the shield wire of the typical audio cable. The two signal lines are inverted with respect to each other. The signal level of the difference between these two signal lines is at line level (which is somewhere between -20dB and +8dB typically).

Differential Linearity Error The Differential Linearity of a D/A conversion system is the measure of the variation of the analog output from the desired value when the digital input is changed by 1LSB. Generally, this measurement is referenced to a specific operating level or normalized to full scale output.

Differential PCM Differential Pulse Code Modulation. A PCM system where the values produced by the A/D converter are compared with the input. This can be a signal fed from a D/A converter placed at the A/D converter output or a delayed (or held) analog voltage.

Dim An attenuation of approximately 40dB used to reduce the monitor volume in order to allow conversation or talkback without totally muting the monitor signals.

Direct Box A device used to convert line level or instrument pick-ups to microphone level signals so that they can be connected to the microphone pre-amplifier inputs of the console. Basically, this is a transformer or resistor network which converts a high impedance unbalanced audio signal into a low impedance balanced audio signal.

Direct Sound Sound travelling directly from the sound source to the listener without reflections.

Distortion Sounds present in the output which were not present on the input, generally causing poor sound quality and derived from improper matching, signal overload, or poor wiring connections.

Dither A low level white noise signal added at the A/D converter stage used to randomize the effects of quantization error and quantization noise. In the analog domain, this is white noise added to the analog input signal. In the digital domain, this is done by randomizing the LSB (synchronized to the conversion cycle).

Dolby Tone A reference tone recorded on a tape which will be encoded with Dolby Noise Reduction used for calibration.

Drop-out A momentary loss of playback signal due to manufacturing defects on the tape, dirty heads, or misadjustments.

Dry A room, recording, or microphone placement which has no echo or reverberation. This may also describe signals that have not been processed or equalized.

Dump Monitor to Bus Dump. A special operation in which the 2-Mix signals are fed to the Channel Bus. Used for moving recorded signals from one track over to the other tracks.

Dynamic Range The range of volume levels in a musical program. This is determined by the difference between the softest and the loudest sounds.

Earth Ground A connection to the earth usually done with a copper rod driven into the ground.

Echo Return A line level return which routes external signals to the stereo buses (2-Mix).

Effects Unit A device, external to the console used for audio signal processing usually adding a special effects to the sound.

Electronic Editing The process of arranging recorded material without physically cutting the tape. This is done for assembling the songs of a project or for joining the best takes of a song.

Electrostatic The presence of static electricity or the force field between Interference two conductors charged with static electricity in a signal conductor causing hum, distortion, and/or excessive noise.

Emphasis Emphasis is an audio conditioning circuit which is incorporated into the analog sections (A/D input and D/A output) of the sampling system. On the input side, a boost of the high frequency content of the analog signal (pre-emphasis) and the writing of the Emphasis bit are realized. On the output side, attenuation of the high frequency content of the analog signal (de-emphasis) is automatically activated when the Emphasis bit (within the digital audio data) is ON.

Envelope The rise and fall in volume of one note. Each harmonic in a complex waveform may have a different envelope.

Equalizer A circuit used to emphasize or suppress some of the audio signals at certain frequencies so as to change the sound characteristics and improve the final mix.

FEX In an APR-5000 Series recorder, the acronym for the Front End Transformer Board.

Fade-out The gradual reduction in volume in the last few seconds of a song. This is usually done by pulling down the audio master or 2-Mix fader to the lowest position.

Fader A gain control.

Feed Used in two ways: 1) a feed is an audio signal output from another system which will be connected to an input, and 2) to feed is to route an audio output to another system.

Feedback The return of some portion of the output signal to the system's input.

Filter A circuit which sharply attenuates signals above (low pass or high cut) or below (high pass or low cut) frequency. These are used to reduce unwanted noise such as hiss or rumble.

Float To disconnect from ground (i.e., a floating output has no ground reference.

Floating Point This is a method of quantizing discrete analog voltages into digital data which has two parts: the exponent and the mantissa. The mantissa describes the analog voltage to a high (or fine) resolution. The exponent describes the gain range. This method is sometimes called "flying comma".

Flutter The deterioration of recorded sound caused by rapid and periodic variations in tape speed.

Foldback See Cue.

Frame	Originally used to describe one picture on a film. A time code frame is based on this principle, each second resolved to either 30 (SMPTE) 29.97 (SMPTE Drop Frame) or 25 (EBU) frames. Also short for console main frame.
Frequency Response Chart	The graph of signal amplitude to frequency. A flat frequency response is obtained when all audio frequencies input to a system at the same level are all output at the same level.
Front Porch	The portion of a video signal that follows the video portion but precedes the negative-going sync pulse.
Full Track	A single tape track recorded across the full width of a 1/4-inch tape.
Fundamental	The lowest frequency in a complex wave.
Gain	Amplification or increase of the signal level.
Gain Riding	The practice of manually adjusting the gain in a signal path resulting in an altered dynamic range.
Generation	An analog copy of a tape. An analog copy of the master tape is a first generation copy. Each analog copy of a copy is reduced by a generation and results in generation loss which is a degradation of sound quality.
Gobo	A movable partition used to isolate microphones. Short for "go-between".
Ground	The zero-voltage reference for electronic circuitry. In the SONY professional mixing consoles, several ground points are used, one for the digital circuitry, one for the indicators, one for the audio circuitry, and a chassis ground.
Guard Band	The spacing between the tracks on a multi-track tape or tape head used to prevent crosstalk.
Hz	Letter symbol for hertz, meaning cycles per second (of any periodic phenomenon).

Half Track A tape where there are two tracks recorded across the full width of the tape (usually 1/4-inch). Also, center track time code machines are half track with the time code recorded in the guard band.

Harmonic An overtone whose frequency is a whole number multiple of the fundamental frequency.

Headroom The difference between the standard operating level and the maximum signal level before clipping or distortion. Since the maximum allowable signal level of a console is determined by its electrical design, the amount of headroom will be determined by the operating level.

Hertz The unit of frequency measurement (1 Hz = 1 cycle per second).

High Pass Filter An audio filter used to attenuate low frequency components of the signal without affecting the mid and high frequency components. Also used to reduce rumble and hum in an analog signal.

Hiss A noise which contained all frequencies but is more predominant at the high end. Hiss sounds like wind blowing or like the sibilance in the word "hiss".

Horizontal Resolution (of a CRT) The horizontal resolution of a TV monitor determined by the bandwidth of the video signal. The bandwidth represents the switching time of the electronic (video) signal. This video signal is the electronic signal which turns the electron beam on and off.

Hot A high recording level or the electrical wire which has the more positive voltage on it (+).

Hum An unwanted low frequency signal, usually related to the power line heard along with the audio signal.

I/O Input/Output module. A module containing all of the circuits and controls between microphone and recorder for a single audio channel (Channel signal path). It also incorporates all of the circuits and controls between the line return and the 2-Mix (Monitor signal path).

IC 1) Abbreviation for integrated circuit.
2) Abbreviation for internal connection.

Image A sound in a stereo mix which seems to be originating from somewhere between the two speakers. The image is controlled by the pan pots.

Insertion The change of a signal level resulting from the connection Gain/Loss of electronic components such as audio signal processors or conditioners.

Interleaving The process of placing data in a different sequence. This is done so that in the event of a burst error where several sequential data words from the storage device are lost, the missing data will interdispersed within the data stream when the data is placed in the original sequence (de-interleaved).

Interpolation A method of recreating missing data by adding the sample values before and after the missing value and dividing by two.

Jack A individual socket or hole in the patch bay.

Jitter A time base distortion usually caused by an unstable tape transport system or improperly synchronized equipment (out of sync). In a video system, this may also be caused by a noisy transmission line.

KBD In an APR-5000 Series recorder, the acronym for the Key Panel Board.

LNT In an APR-5000 Series recorder, the acronym for the Local/Network Transceiver Board.

Leader	Plastic or paper tape which has no oxide and is used for separating songs on an analog tape or also used at the beginning and end of magnetic tape for easier threading.
Leakage	Extraneous sounds or noises unintentionally introduced into an audio system. Mostly, this describes sound indirectly picked up by a microphone.
Limiters	A compressor whose output remains constant regardless of the input signal level.
Linear Fader	A slider-type gain control.
Line Level	A signal whose level is between (approximately) -10dBm and +4dBm.
Live	A room, recording, or microphone placement which has audible ambient reverberation. Also used to indicate that an event is occurring in real time or in person.
Localization	The ability of the human ear to determine the direction of a real sound source or a stereo image.
Lock	Indicates a fully synchronized system. In the case of video equipment, this indicates that the drums are locked to their (common) reference or sync signal. In the case of audio recorders, this indicates that they are synchronized by way of signals recorded on the tape (and the playback of these signals are in sync). The synchronizing signal on an audio tape machine will be time code (or CTL in the case of the DASH digital audio machines).
Low Pass Filter	An audio filter used to attenuate high frequency components of the signal without affecting mid and low frequency components. For the A/D conversion process, a LPF is used to attenuate frequencies which are greater than the Nyquist frequency. In the D/A conversion process, a LPF is used to remove the effects of quantization error. The general audio usage is to reduce hiss.

MSB In an APR-5000 Series recorder, the acronym for the Signal Muting Board.

MST In an APR-5000 Series recorder, the acronym for the Audio Master Card.

MST-II In an APR-24 Series recorder, the acronym for the Audio Master II Card.

Master Module A module containing all of the return controls and the Master summing amplifiers for the final recorded mix.

Monitor The signal flow path monitored to the operator. Sometimes called the 2-mix.

Monitor Module A module containing the circuits used for control room and studio monitoring.

Mono Mix A monaural signal derived by mixing the left and right components of a stereo signal.

Monotonicity A D/A converter measurement of accuracy. If the digital input increases but the output remains constant, the D/A converter is monotonic. This is also related to the differential linearity error.

Multi-track A tape recorder with multiple tracks usually 8, 16, or 24 channels.

Mute Disconnection of the audio source.

Noise Any unwanted audible signals. Ambient noise is the long term noise in a specific environment. Quantization noise is caused by errors in the sampling process.

Noise Gate A device which mutes its signal path unless there is an audio signal present of a certain predetermined level (threshold). A noise gate is an expander whose threshold is set to eliminate rumble, leakage, etc.

Noise Reduction System	An audio conditioning system, these devices are not intended to change the audio signals, they are basically used to improve the transmission medium (usually a tape machine or transmitter).
Notch Filter	A filter which affects only a narrow band of frequencies.
Nyquist Frequency	This is one half of the sampling frequency and describes the highest frequency that can be sampled. Sampling frequencies that are higher than one half of the sampling frequency results in alias frequencies in the audio bandwidth.
Nyquist Rate	This is the sampling frequency required to sample analog waveforms within a given range of frequencies. It is twice the highest frequency that must be sampled. Half of the Nyquist rate (F_s) is called the Nyquist frequency.
Pan	Panning is the process used to shift the apparent left-right position, or image, or a sound source. This originates from the film industry terminology "panorama".
Pilot Tone	A very stable signal used as a reference for synchronization of electronic equipment. This signal is either a squarewave (or sinewave) at a frequency of 50Hz or 60Hz.
Polarity	Refers to the positive or negative direction of a magnetic or electrical force.
Pre-Emphasis	This is the emphasis circuit used on the input of the A/D converter. It is enabled by the user to provide a boost of the high frequency content of the analog signal.
Pulse Code Modulation	This is the method of transforming analog signals into a digital data format and storing that information on a storage system such as magnetic tape or optical disk.

Quantization The process of converting infinitely variable (analog) voltages to specific values within a finite range. This is the process which introduces error into the sampling system because any single value will describe a range of analog voltages regardless of how many (finite) different values are available. Of course, as the number of different values available increases, the range of analog voltages described by each one decreases, therefore, an increase in the number of bits used will result in a (geometric) increase in precision of the sampling system.

Quantization Error The quantization error is the difference between the analog input signal and the digital representation of that signal. It is caused by the fact that each digitized value represents a range of analog voltages and is a function of the number of bits used to describe the analog voltage.

Quantization Noise The quantization noise is the effect of quantization error. It is more noticeable for low level signals than for high level signals which implies a signal-to-quantization noise ratio for any sampling system.

RMD In an APR-5000 Series recorder, the acronym for the Reel Motor Driver Board.

RMD-II In an APR-24 Series recorder, the acronym for the Reel Motor Driver II Board. The circuit design of this board is similar to the design used for the RMD board. The differences are required due to the higher output demand of the 2-inch tape transport of the APR-24.

RTS (RTS-1) In an APR-5000 or APR-24 Series recorder, the acronym for the Reel Tachometer Sensor Board.

Release Time The recovery time of a compressor or expander to nominal gain after gain reduction has been achieved.

Retrace A part of a video signal which occurs while the beam sweeps from one edge of the screen to the other or during the time that it returns from the bottom to the top. Since the beam is turned off during this time, all of the synchronizing information is placed in this portion of the video signal.

SBR In a limited number of APR-5002 Series recorders (serial #20001 to 20700), the acronym for the Silicon Bridge Rectifier Board.

Sends Auxiliary audio outputs from the console normally used to drive cue amplifiers and echo chambers or other external effects devices.

Settling Time The time it takes for an output to stabilize to within a certain deviation from the desired output value. For instance, the output of a TTL logic device may contain transient switching noise for a short period of time as it changes state. This is called the settling time, during this time the output is relatively unstable and unuseful.

Signal-to-Noise A commonly used term to describe the difference between the typical operating audio signal level and the fixed noise floor (s/n ratio) of a given piece of audio equipment. Generally, this measurement is taken using a weighting filter. One of the methods of defining the Signal-to-Noise Ratio for digital audio equipment is to calculate the difference between the full scale output and the output with no signal applied.

Skew Bits In the Composite Digital recording format, these bits are used for control information storage. Information such as sampling frequency and emphasis ON/OFF are presently utilized. There are 35 skew bits per interleave block of digital audio data. 33 of these bits are reserved for future expansion.

Slate Talkback to the 2-Mix or tracks used to identify a particular recording. Also a low frequency audio signal recorded on tape (together with Slate Talkback) as a Take marker. This originates from the film industry practice using a chalk and slate.

Slate Osc The oscillator which generates the low frequency Slate tone.

Solo The opposite of mute. When this mode is activated, all of the other audio inputs will be muted causing the SOLOed signal to be heard exclusively.

Special Effects This describes outboard equipment used for sound sweetening. Generally these devices are used for creative purposes causing the sound texture to be changed. Examples of special effects devices are phasors, flangers, chorus, doublers, octavers, etc.

Spectrum Analyzer A device which displays the distribution of frequencies. The range of an audio frequency spectrum analyzer is 20Hz to 20kHz.

Splice Editing The process of cutting and splicing magnetic tape in order to delete unwanted material, insert leader tape between songs, or to rearrange recorded material to the desired order.

Stereo The common abbreviation for "stereophonic sound". This is a sound system which consists of several microphones and pairs of loudspeakers. Two separate signals are simultaneously incorporated to create the stereo effect. The channels are labelled right and left corresponding with the loudspeaker positioning. Notice that this is not the same as binaural sound.

Sub-carrier The portion of the video signal which carries the color information. This is a continuous wave signal that constitutes the color part of every picture frame. A pure sub-carrier has a frequency of 3.58MHz, the phase of which determines the color of the picture at any given point (as processed by the encoder). A small section of the sub-carrier is placed on every video line (color burst in the back porch area).

Successive Approximation Register This is a form of A/D conversion. An analog voltage is presented on the input approximation register (SAR) which compares the analog voltage with a reference level. At first this will be the halfway point between the maximum input voltage (1111...) and the minimum voltage input (0000...). If the voltage is the same or higher than the median, a bit is set ON and the reference is increased to the halfway point between the maximum and the previous reference level (in this case the median). If the voltage is lower than the reference, a bit is turned OFF and the reference is decreased to the halfway point between the minimum level and the previous reference level. This process continues until all bits have been set.

Suppress To mute or attenuate.

Sync A synchronizing pulse. 3/4-inch VTR units used for digital mastering use composite video as a sync source.

Synchronize To lock one element of a system into step with another through the use of a common signal. For example, two tape machine servo systems referenced to a time code signal.

Synchronization The precise matching of two (or more) machines to a common reference signal (i.e. time code, composite sync, pilot tone).

Syndromes These are error status signals which are activated to indicate errors in the digital audio data as detected by the error detection circuitry.

TCC In an APR-5003/5003V Series recorder, the acronym for the Time Code Channel Board.

TCM In an APR-5003/5003V Series recorder, the acronym for the Time Code Channel Meter Board.

THD+N Total Harmonic Distortion plus Noise is defined as the ratio of the sum of the squares of the values of the harmonics and noise to the fundamental input frequency. This is most often expressed as a percentage (%). Note that the distribution and amplitude of the various noise, error, and distortion components varies with the operating level of the equipment under test. Therefore, in order to be effective or useful, the THD+N measurement should be performed for several different input signal levels including the typical operating level range.

TIB In an APR-5000 or an APR-24 Series recorder, the acronym for the Transport Interface Board.

TTS In an APR-5000 or an APR-24 Series recorder, the acronym for the Tape Tachometer Sensor Board.

Talkback An operational mode which allows the console operator to talk directly to the studio loudspeakers or to headphones.

Time Code A self-clocking signal used to provide timing reference to magnetic tape. The purpose of the time code signal is to provide electronic sprocket holes or specifically described time signatures to the tape. The most popular forms of time code are SMPTE (30 frames/second), SMPTE DF (29.97 frames/second), EBU (25 frames/second), and FILM (24 frames/second).

Two (2)-Mix The stereo program output. Sometimes called the monitor mix.

VCA Voltage Controlled Amplifier. An amplifier whose gain is controlled by varying the DC voltage applied to one of its input terminals.

VCO Voltage Controlled Oscillator. An oscillator whose output frequency is controlled by varying the DC voltage applied to one of its input terminals.

VITC The letter abbreviation for Vertical Interval Time Code.

VVT In an APR-5003V or an APR-24 Series recorder, the acronym for the Video/VITC Translator Board.

Vertical Resolution (of a CRT) The vertical resolution of a TV monitor is defined by the number of lines that are electronically generated.

Walsh Radiator A type of speaker driver invented by Lincoln Walsh, in which a gently sloping cone, moving up and down, so displaces the air with its sloped sides as to radiate a cylindrical wavefront in a 360-degree horizontal circle.

Waveshape A graph of a wave as a function of time or distance.

Word A set of bits used to describe a value. The set of bits as a composite is known as a digital word.

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APPLICATION NOTES

NOTE 1

SERIAL CONTROL WITH SONY BVE-900 and BVE-9000 EDITORS

GENERAL COMMENTS

The general behavior of the APR-5003V as a source machine is similar enough to that of a VTR as to be largely transparent to the operator. The machine's handling of time code, manual transport controls, and source selection in an edit appears to be virtually the same as normal VTR operation, but, because of limitations in editor architecture, certain edit types may require Mixer Setup changes.

Operation of the ATR with the editor does not utilize the ATR's CHASE, or other higher order features such as PREVIEW, EDIT or REVIEW. The editor simply instructs the ATR to shuttle and stop at specific points. VARIABLE SPEED PLAY commands provide the means to position the ATR to be synchronous before the IN POINT is reached. Once the correct synchronous operation is attained, the ATR is commanded to RESOLVE to the external video reference. The editor is the sole controlling entity in the process of the edit sequence.

CONNECTIONS AND SETUP

For proper serial control with SONY BVE-900 and BVE-9000 Editors, the following conditions must be met.

1. The Editor must be connected to the APR-5003V via the **TRIBUTARY** serial port on the rear panel of the machine. (See Figure 1.)
2. The house video reference must be connected to either one of the **VIDEO** ports on the rear panel, and the **TERMINATION** switch must be set as follows:
 - a. Where the APR-5003V is the video reference terminating link, the switch must be set to **ON**.
 - b. Where the video reference is daisy-chained to another device, the switch must be set to **OFF**.
3. Storage Location 37 must be set to 1, thereby selecting video as the resolving reference.
4. The correct tape speed must be selected relative to the Time Code on tape, and a consistent Time Code type must be used throughout the system.
5. The Setup Menus for VTR BLOCK #1 and VTR BLOCK #2 must be in accordance with the data given in the **Recommended Menu Setup for ATR usage as Player** section given later in this document.

It should be noted that, at power-up, the Editor disables the machine's local control with its initial commands. This can be re-established by pressing the **LOCAL** key on the Transport Control Panel. Furthermore, the serial control capability can be disengaged by deselecting the **NETWORK** key on the same panel.

METHODS OF USE

Stand Alone, Audio Only, Source Edits

In this application, the ATR operates as a stand-alone audio source, and programming an edit does not differ from normal VTR operation. Specifically, an audio only Cut or Dissolve from the ATR is programmed in the same manner as it would be for a video source. The ATR is not linked with any other Player. Time Code match frames are listed in the same manner as with VTR applications. Edit data for the ATR is preserved in the EDL.

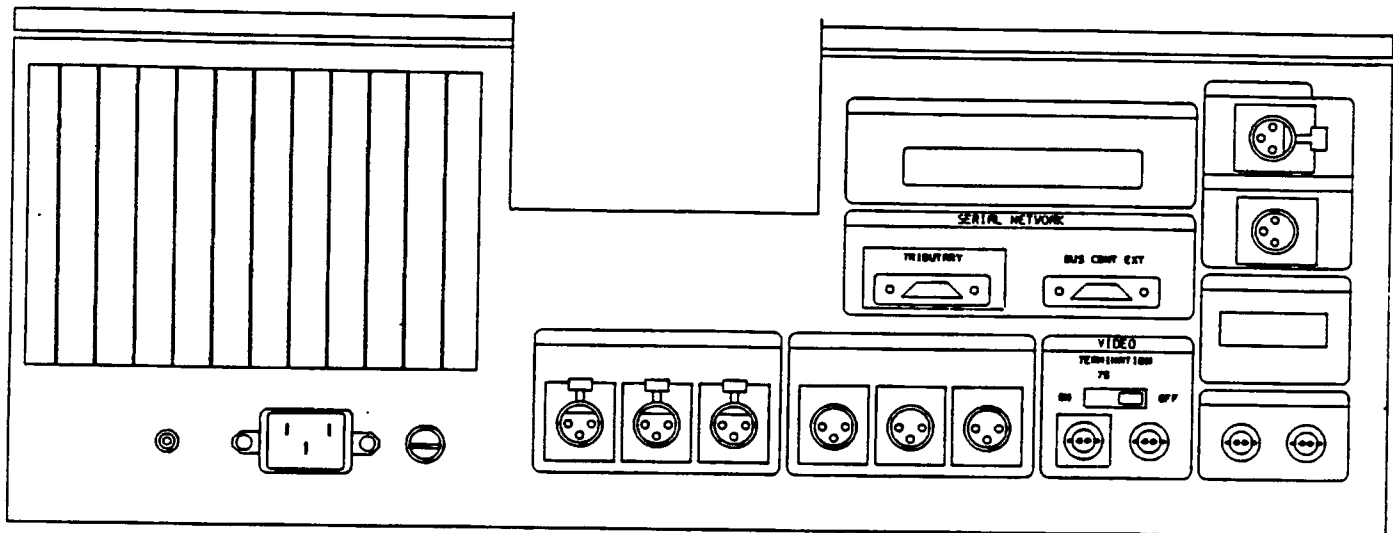


Figure 1. Rear Panel Connectors

Effect Type (Manual)

A Manual effect type allows the operator to choose a background and a foreground source for the edit. Selecting the ATR as the background source and a VTR as the foreground source allows the user to record Video from the VTR while recording audio from the ATR. Edit data relative to each source is preserved in the EDL. This application is most suitable for matching "sync-sound" with previously recorded video material.

CAUTION: Audio from the Foreground (VTR) source also is present in this edit unless the Fader associated with this player is muted or faded down.

ATR as Audio Source in a Cut with Video from another Player

This is an alternate method to the Effect Type (Manual) for combining audio from the ATR with Video from a player ATR. This method requires the manual re-assignment of the Mixer cross-points in the BVE-900 Setup menu, as follows:

Mixer Block Reassignment

The Mixer Block Setup identifies for the editor the interconnections between mixer inputs and player outputs, i.e. which input channels of the mixer are connected with which output signals of the players. In this application, the user will simply exchange the identities of the audio and video sources so that the editor controls the ATR Fader as if it were the audio from the designated Video source.

Depending upon the mixer and its configuration, each cross-point assignment represents either two Mono Faders or one Stereo Line Input Fader. The SONY MXP-29 will always provide two Mono channels for each source. The SONY MXP-2000 can be configured either for dual Mono Fader operation, or can be configured with a single Stereo Line Input channel for each player.

EXAMPLE:

Initial Assignment:

P1 is designated Video Source Byte #2 assigned "01" (hex)

P3 is selected Audio Source (ATR) Byte #4 assigned "03" (hex)

Assignment Exchanged:

P1 is designated Video Source Byte #2 assigned "03" (hex)

P3 is selected Audio Source (ATR) Byte #4 assigned "01" (hex)

In this example, P1 is designated as the source of the edit. P3 should be selected with an asterisk "*" to assign the tandem roll of the ATR with P1. The ATR's Fader should be set to the desired level. The P1 VTR Fader position will have no effect on the audio edit. The P3 (ATR) Fader will be controlled by the editor as if it were the P1 (VTR) Fader.

It is very important to realize that no indication will appear in the EDL to identify P3 as the audio source in this edit.

ATR as Audio Source in a Dissolve or Wipe

The following examples illustrate situations in which one VTR's (P1) sync-sound is located on an ATR (P3).

Two Event Method:

The first event is programmed as a video only transition effect between P1 and P2. This preserves the video edit data in the EDL. The edit data specific to this event needs to be manually brought forward for use in the second event. The second event is programmed as an audio only transition effect between the P3 (ATR) and P2. This would register the sync-sound audio edit data in the EDL, thus providing sufficient data for the operator to re-create this edit sequence. The Mixer cross-points need not be reassigned when using this technique.

Single Event Methods:

General Notes

The Single event techniques identified below require that Mixer cross-points be reassigned. Please refer to the section above on "Mixer Block reassignment".

It also is helpful to remember that, in any effect, by selecting the ATR (P3) with an asterisk "*", the ATR is thus selected to perform a tandem roll with the first source in the edit process.

Match Frame; ATR in Tandem roll with "From" or "To" Machine

In this example, the P1 VTR is the video source whose sync-sound is located on the P3 ATR. A match frame transition effect from P1 to P2 or from P2 to P1 would be programmed in the customary manner, with the additional requirement that a tandem roll with the ATR be invoked by means of the asterisk "*" selection.

It is important to ensure that P1's mixer block assignment is exchanged with that of the P3 ATR. After the edit is complete, the assignment may be returned to its original settings.

As in any edit where the mixer block is reassigned, this setup information will not appear in the EDL, neither will P3's participation in this edit be preserved.

Delayed Transition; ATR in tandem with "From" Machine

In this example, the P1 VTR is the video source whose sync-sound is located on the P3 ATR. A delayed transition effect from P1 to P2 would be programmed in the customary manner, with the additional requirement that a tandem roll with the ATR be invoked by means of the asterisk "*" selection.

It is important to ensure that P1's mixer block assignment is exchanged with that of the P3 ATR.

After the edit is complete, the assignment may be returned to its original settings.

As in any edit where the mixer block is reassigned, this setup information will not appear in the EDL, neither will P3's participation in this edit be preserved.

Delayed Transition; ATR in tandem with "To" Machine

In this example, the P1 VTR is the video source whose sync-sound is located on the P3 ATR. A delayed transition effect from P2 to P1 would be programmed in the customary manner, with two additional requirements.

First, that a tandem roll with the ATR be invoked by means of the asterisk "*" selection.

Second, that the duration of the P2 edit ("From machine") be subtracted from the P3 (ATR) IN POINT. Remember, by selecting the ATR (P3) with an asterisk "*", the ATR is selected to perform a tandem roll with the first source in the edit process.

Again, it is important to ensure that the P1 Mixer Block assignment is exchanged with that of the P3 ATR. After the edit, the assignment may be returned to its original settings.

As in any edit where the mixer block is reassigned, this setup information will not appear in the EDL, neither will P3's participation in this edit be preserved.

Other restrictions to the use of the APR-5003V as a Player

The APR-5003V will not perform a synchronous DMC edit. The APR cannot provide synchronous and frame accurate operation with video at anything other than normal forward speed. However, if the ATR is assigned a sync grade of "Preroll and Play" (SYC4) the ATR will accept and perform a programmed DMC edit in the forward direction only. The APR-5003V will allow audio monitoring at DMC variable speeds in the forward direction without any special Auxiliary Menu changes.

When using the APR-5003V with the BVE-9000 Editor, the Editor VARI-SCAN argument should never be such as to cause a play speed greater than 100% of its nominal value, this argument being set in a machine-specific manner through the use of the DMC RANGE setup window.

Under certain conditions, the rapid rotation of the supply reel cannot be decelerated at the rate commanded by the Editor, and it is possible for the user to switch between STOP, a fast VARI-SCAN speed, and the normal PLAY speed in a sequence so rapid as to prevent the APR-5003V from performing in a manner befitting its excellent tape handling characteristics. Because of this physical tape transport limitation, the following change in the DMC RANGE setup is recommended.

STEP 1. Select the ATR.

STEP 2. Select the DMC RANGE setup window.

STEP 3. Press Function Key F4.

STEP 4. Enter "100" via the Numeric Keypad.

STEP 5. Press "ENTER".

Use of the BKE-9601 (Time Code Generator/Reader) in conjunction with its parent BKE-9600 (Intelligent Device Controller) is not recommended for APR-5003V control purposes, since this combination does not support Macro-cue facilities with the BVE-9000 Editor.

For best results, 15 ips tape speed should be used with SONY BVE-900/9000 Editors. 30 ips has good performance, but program duration is limited by the rapid rate of tape usage. In addition, LOCATE times become longer at 30 ips. At 7.5 ips operation the editor is at somewhat of a disadvantage in that, in pursuit of synchronization, the editor's control actions tend to compromise Time Code read integrity. Thus, while both 7.5 and 30 ips speeds are fully functional, the best combination of fidelity, tape utilization, and locking integrity is realized at 15 ips operation.

Recommended Menu Setup for ATR usage as Player.

"VTR BLOCK #1" SETUP MENU

		NTSC Settings		PAL settings	
Byte 1	(Device Type)	01010000	50	01010000	50
Byte 2	(Device Type)	00000000	00	00000000	00
Byte 3	(Preroll Duration)	00000001	01	00000000	00
Byte 4	(Preroll Duration)	00101100	2C	11111010	FA
Byte 5	(Edit Delay)				
	For 30 ips	00000011	03	00000011	03
	For 15 ips	00000100	04	00000100	04
	For 7.5 ips	00000110	06	00000110	06
Byte 6	(EE Delay)	00000001	01	00000001	01
Byte 7	(Overrun):				
	For 30 ips	00001011	0B	00001010	0A
	For 15 ips	00000111	07	00000110	06
	For 7.5 ips	00001011	0B	00001010	0A
Byte 8	(Trajectory Const)				
	With BVE-900 Editor				
	For 30 and 15 ips	00111111	3F	00111111	3F
	For 7.5 ips	00010101	15	00010101	15
	With BVE-9000 Editor				
	For 30 and 15 ips	10111111	BF	10111111	BF
	For 7.5 ips	10010101	95	10010101	95

"VTR BLOCK #2" SETUP MENU

		NTSC Settings		PAL settings	
Byte 1	(TC Read Delay)	00011111	1F	00011010	1A
Byte 2	(Start Delay):				
	For 30 ips	00001101	0D	00001011	0B
	For 7.5 and 15 ips	00001011	0B	00001010	0A
Byte 3	(After Sync Delay -)	11111101	FD	11111101	FD
Byte 4	(After Sync Delay +)	00000010	02	00000010	02
Byte 5	(Max Framing Enable)	00000000	00	00000000	00
Byte 6	(CF Status Enable)	01111000	78	01111000	78
Byte 7	(Pre roll speed)	00001010	0A	00001010	0A
Byte 8	(Quick Preroll)				
	With BVE-900 Editor	n/a		n/a	
	With BVE-9000 Editor	00111011	3B	00111011	3B

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**APPENDIX C
SMPTE TIME CODE
INFORMATION**

C.0 Overview

This section is a brief outline of general time code information. Reference to this section will promote a more comprehensive understanding of the basics of the present time code format.

C.1 Time Code Background

Originally standardised by the Society of Motion Picture and Television Engineers (SMPTE) for use in videotape editing, time code is a digitally-encoded signal of succedent Hours, Minutes, Seconds, and Frames. It provides time-based reference points on audio and video tape similar to sprocket holes on film. When recorded on one tape source, it can be used for locating, synchronising, and editing purposes with other time code sources.

C.1.1 Time Code Types and Formats

There are two types of time code, Longitudal Time Code (LTC) and Vertical Interval Time Code (VITC).

LTC is recorded on audio or video tape on a separate audio track, and contains 80 bits of information per time code word. When LTC is recorded onto video tape, each frame of the video signal is labeled with its own unique time code word which identifies that particular frame in terms of Hours, Minutes, Seconds, and Frames.

VITC is recorded on video tape in the vertical blanking interval portion of the video signal, and contains 90 bits of information per word.

The two time code types can be in one of four formats, European Broadcasting Union (EBU), SMPTE Non-Drop Frame (NDF), SMPTE Drop Frame (DF), or FILM. Each format is designed for use in a specific application, to wit:

- EBU is used for videotapes made at a rate of 25 frames per second (Fr/s), in accordance with European broadcasting standards;
- SMPTE NDF is used for monochrome videotapes made at a rate of 30 Fr/s, in accordance with National Television Standards Committee (NTSC) standards;
- SMPTE DF is used for color videotapes made at a rate of 29.97 Fr/s, in accordance with NTSC color television standards;
- FILM is used for motion pictures made at a rate of 24 Fr/s.

C.1.2 SMPTE DF

The APR-5003V records SMPTE NDF and SMPTE DF time code at a frequency of 2400 bits per second (80 bits LTC x 30 Fr/s). However, in order to accommodate the slightly less than 30 Fr/s color videotape frame rate of 29.97, two frames are dropped from the SMPTE DF data stream each minute (with the exception of every tenth minute) to correct the offset error that occurs because of the frame rate differential. The short term time error experienced by this format is illustrated in Figure C-1.

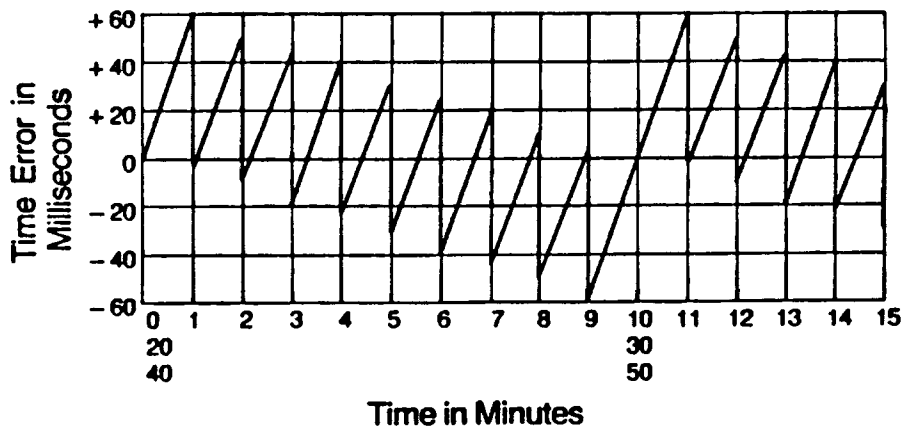


Figure C-1. Short Term Error in Drop Frame Mode

C.1.3 The Time Code Word

The time code word is a digitally-encoded signal of succedent Hours, Minutes, Seconds, and Frames. Before encoding, the 80-bit LTC word is a square wave pulse train of 40 positive and 40 negative excursions, with each bit having a digital value of 0. When the voltage level is switched in the center of the bit, as shown in Figure C-2, it generates a 1/2 bit and assigns that bit with a digital value of 1.

The 80 bits of the LTC word are divided as shown in Figure C-3. In this example, bits 1 and 2 of the Frames Units count switched their voltage level in the center of the bit clock, and therefore have a digital value of 1. As these bits represent the numbers 1 and 2, respectively, of the Frames Units count, adding them together produces a Frames count of a 1 and a 2. The Frames Tens count shows bit 09 being toggled. This will yield a value of 20. Hence, as shown in Figure C-3, the Frames Units code is calculated by the following formula:

$$1 + 2 + 20 = 23\text{rd Frame}$$

Continuing on in this manner to the Seconds, Minutes, and Hours bits, the time code word in this example can be derived to have a value of 16 Hours, 47 Minutes, 31 Seconds, and 23 Frames.

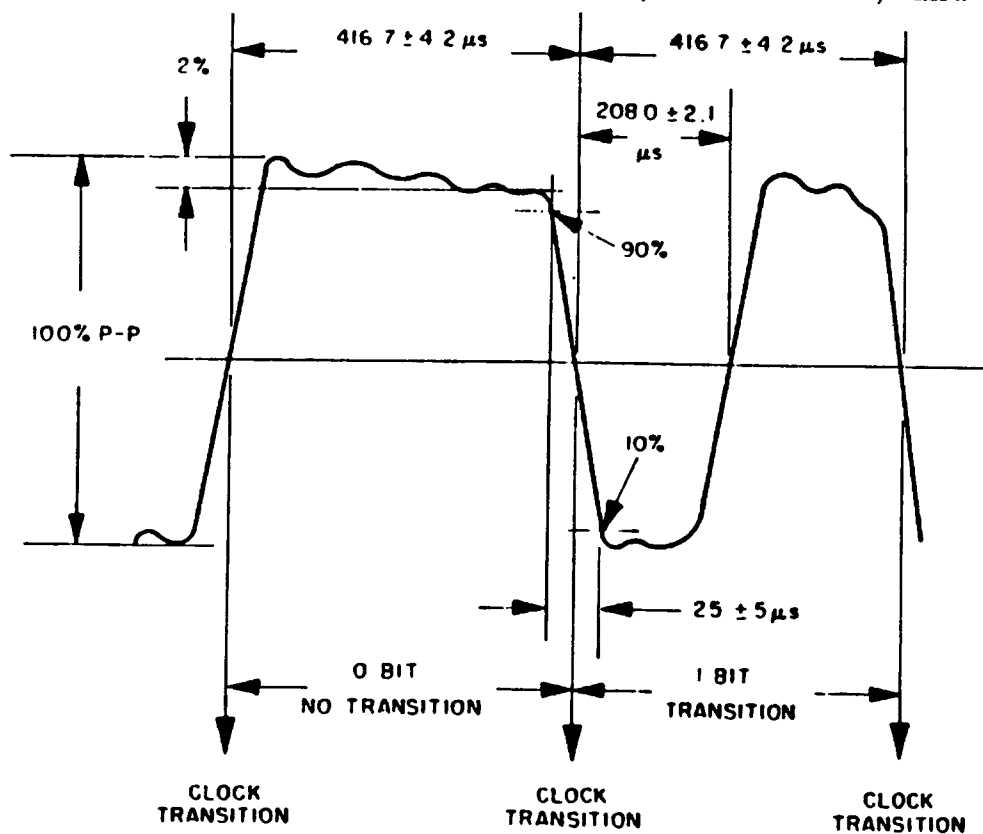


Figure C-2. Time Code Bit Values

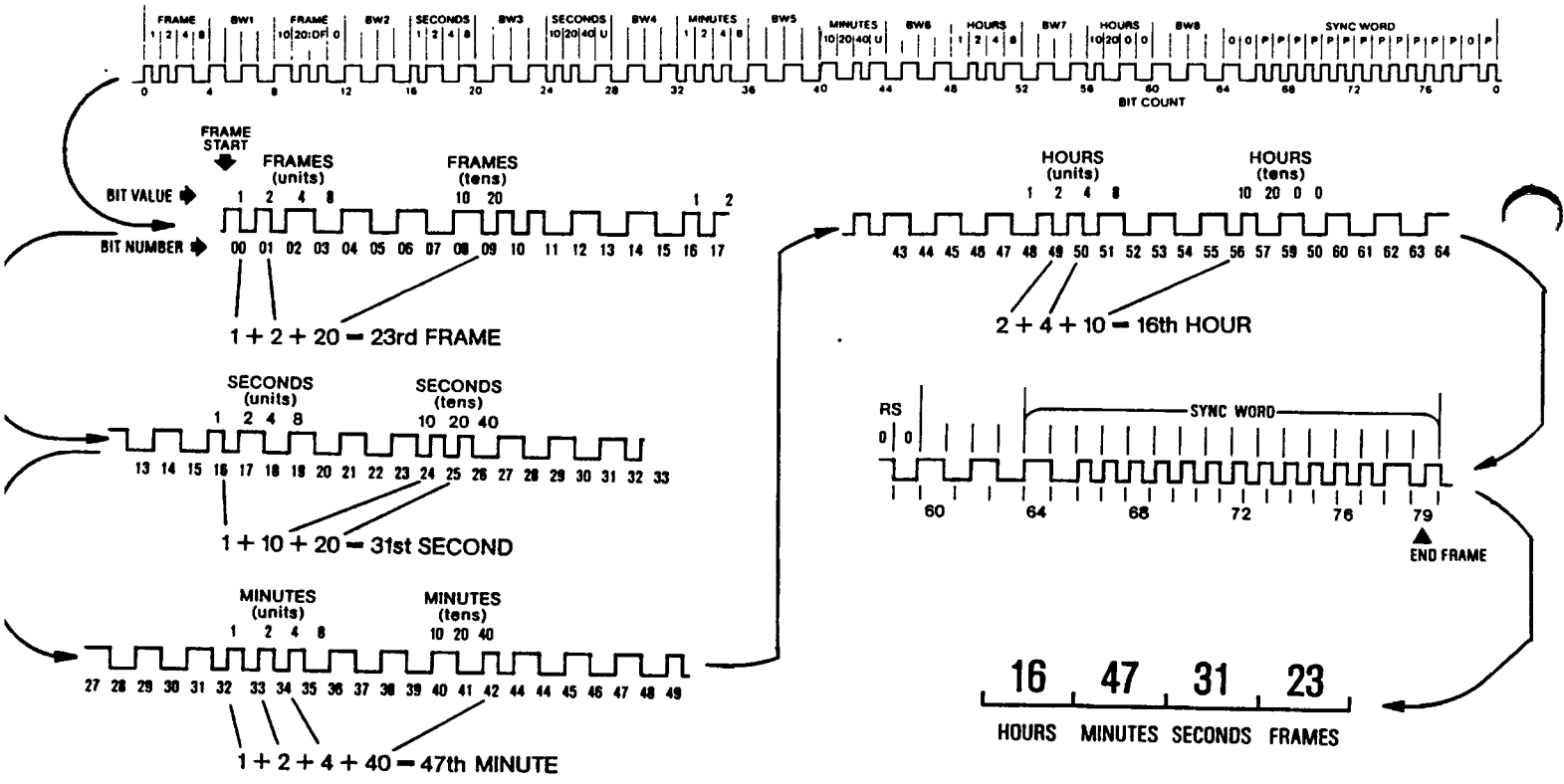


Figure C-3. LTC Word Bit Assignments

The time code word also has several other bits and groups of bits within the data stream for other encoding purposes.

Eight groups of four User Bits are interspersed between the various time code counter bits. The User Bits are all set to 0, and are available for whatever auxiliary encoding that the user might want to assign to them. It should be noted that the APR-5000 does not generate or display User Bits, as this must be done by an external time code generator. The machine does, however, record and output the bits in the same manner as any other bits in the time code word.

Bit 10 is called the Drop Frame Bit. Time code generated in Drop Frame format is identified by having this bit set to a digital 1. Bit 11 is the Color Frame Bit, and when set to a digital 1 it indicates that color frame identification has been applied to the time code signal.

Bits 64 through 79 comprise the Sync Word. The Sync Word is detected by an external time code reader as the end of the time code word. It is also used by an external reader to determine whether the tape is running in the forward or reverse direction. These sixteen bits will always have the same value in every LTC word.

C.1.4 VITC Time Code

The VITC word has ten bits more than the LTC word. Two Sync Bits are placed before each of the numbers count bits, bit 35 is the Field Mark Bit which allows VITC readers to index each video field, and, in place of the sixteen bit Sync Word found at the end of the LTC word, VITC has an eight bit Cyclic Redundancy Check (CRC) error detection code at the end of each word. The comparison of LTC code to VITC code is illustrated in Figure C-4.

VITC

Longitudinal Time Code

VITC BIT NO				BIT NO
0	-1	SYNC BIT		
1	-0	SYNC BIT		
2		1	1	0
3		2	2	1
4		4	4	2
5		8	8	3
6				4
7				5
8				6
9				7
10	-1	SYNC BIT		
11	-0	SYNC BIT		
12		10	10	8
13		20	20	9
14				10
15				11
16				12
17				13
18				14
19				15
20	-1	SYNC BIT		
21	-0	SYNC BIT		
22		1	1	16
23		2	2	17
24		4	4	18
25		8	8	19
26				20
27				21
28				22
29				23
30	-1	SYNC BIT		
31	-0	SYNC BIT		
32		10	10	24
33		20	20	25
34		40	40	26
35				27
36				28
37				29
38				30
39				31
40	-1	SYNC BIT		
41	-0	SYNC BIT		
42		1	1	32
43		2	2	33
44		4	4	34
45		8	8	35
46				36
47				37
48				38
49				39
50	-1	SYNC BIT		
51	-0	SYNC BIT		
52		10	10	40
53		20	20	41
54		40	40	42
55				43
56				44
57				45
58				46
59				47
60	-1	SYNC BIT		
61	-0	SYNC BIT		
62		1	1	48
63		2	2	49
64		4	4	50
65		8	8	51
66				52
67				53
68				54
69				55
70	-1	SYNC BIT		
71	-0	SYNC BIT		
72		10	10	56
73		20	20	57
74				58
75				59
76				60
77				61
78				62
79				63
80	-1	SYNC BIT		
81	-0	SYNC BIT		
82				64
83				65
84				66
85				67
86				68
87				69
88				70
89				71
				72
				73
				74
				75
				76
				77
				78
				79

Figure C-4. VITC Code vs LTC Code

APPENDIX D

APR-5000 SERIES JUMPER/SWITCH LOCATION AND FUNCTION

D.0 Overview

This appendix covers the many jumpers and DIP switches locally mounted on each PC board of the APR-5000 Series recorders. All PC boards are listed in alphabetical order for service engineer reference. Included with each jumper listing is a brief description of what function the jumper serves.

D.1 APR-5000 Jumpers and Switches

D.1.1 ACM Board

For these descriptions, refer to Figure 7-3 on page 7-5 of this manual. There are three jumper wires located on the ACM board. The descriptions of these jumpers are listed below:

- JW-1** : Normally OUT on the APR-5000 Series, this jumper is used for the PCM-3102/3202 models. Since the APR Series uses only one speaker, this jumper is removed. When installed, this jumper will direct the RIGHT AUDIO RETURN from the headphone connector (CNJ-221) to the right side speaker (mounted in the Meter Bridge).
- JW-2** : Normally IN on the APR-5000 Series, this jumper connects the LEFT AUDIO RETURN from the headphone connector (CNJ-221) to the right side speaker (mounted in the Meter Bridge). When this board is installed into a PCM-3102/3202, this jumper is removed and JW-1 is installed.
- JW-3** : Normally OUT on the APR-5000 Series, this jumper (when installed) will connect the CH1 and CH2 meter signal feeds together. This allows a constant signal connection to the MUTE switch (DG-212) IC1.

D.1.2 ADM Board

There are no jumpers or switches located on this board.

D.1.3 ALN Board

There are no jumpers or switches located on this board.

D.1.4 CNL Board

For these descriptions, refer to Figure 7-10A and 7-10B on pages 7-13 and 7-14 of this manual.

- JW-1** : Normally OUT on the APR-5000 Series, this jumper (when installed) will connect the "COLD" lead of the REPRO head to ground. This connection will perform a hard wire single ended signal being returned from the REPRO head. This jumper is not used on any revision of the CNL card.
- JW-2** : Normally IN on the APR-5000 Series, this jumper connects the BIAS signal output (pin 8 of K2) to the edge connector pin 5A.
- JW-3** : Normally IN on the APR-5000 Series, this jumper connects the ERASE signal output (pin 3 of K2) to the edge connector pin 6A.
- JW-4** : Normally IN on the APR-5000 Series, this jumper connects the REC ON N (SYNC N) signal output (collector pin of Q1) to the edge connector pin 34B. This command line is directed to the FEX board for switching control of the FEX relay for channel n. The command will switch the relay on the FEX board to either feed record drive signal to the head, or receive playback signal from the head.
- JW-5** : Normally OUT on the APR-5000 Series, this jumper (when installed) connects the REC ON N (REC ON) signal output (collector pin of Q8) to the edge connector pin 34B. This configuration will a similar operation to that of JW-4.

D.1.5 CNX Board

For these descriptions, refer to Figure 7-12 on page 7-16 of this manual. The configuration of JU-1, JU-2, JU-3, and JU-4 are at the operators discretion. The APR-5000 Series machines have the capability of either an analog differential line output or an RS-422 output for the LTC port. The normal factory configuration is JU-1 and JU-3 installed. If a change to the output stage of the LTC signal is desired, follow the guidelines shown in the jumper descriptions that follow. JU-5 and JU-6 are mutually exclusive.

- JU-1** : Normally IN on the APR-5000 Series, this jumper (used in conjunction with JU-3) connects the High side of the DLO (Differential Line Output) hybrid (IC14) to the LTC OUT connector on the rear panel. If this jumper is used, JU-3 MUST be installed.
- JU-2** : Normally OUT on the APR-5000 Series, this jumper (used in conjunction with JU-4) connects the High side of the RS-422 output driver (IC16A pin 2), a 26LS31, to the LTC OUT connector on the rear panel. If this jumper is used, JU-4 MUST be installed.
- JU-3** : Normally IN on the APR-5000 Series, this jumper (used in conjunction with JU-1) connects the Low side of the DLO (Differential Line Output) hybrid (IC14) to the LTC OUT connector on the rear panel. If this jumper is used, JU-1 MUST be installed.
- JU-4** : Normally OUT on the APR-5000 Series, this jumper (used in conjunction with JU-2) connects the Low side of the RS-422 output driver (IC16A, pin 3), a 26LS31, to the LTC OUT connector on the rear panel. If this jumper is used, JU-2 MUST be installed.
- JU-5** : Normally OUT on the APR-5000 Series, this jumper (used in the PCM-3102/3202 machines only) connects the ANA REC READY line from pin 12 of IC6 (74LS373 Octal D-type flip/flop w/output enable) to pin 7 of the 50-pin parallel port (of a PCM-3102/3202). This jumper is ONLY installed on PCM-3102/3202 models.
- JU-6** : Normally IN on the APR-5000 Series, this jumper connects the ERASE OFF 2 line from pin 12 of CNJ-451 to pin 7 of the 50-pin parallel port (of an APR-5000). This jumper is ONLY installed on APR-5000 models. This jumper allows channel status information for the time code channel ERASE LED (located on the RM-5010 remote controller).
- JU-7** : Normally OUT on the APR-5000 Series, this jumper (used in the PCM-3102/3202 machines only) connects the ground to capacitors C5 and C6. This enables the function of the low pass filter configuration of R18, R19, C5 and C6 ($F_c=100\text{kHz}$). This jumper is ONLY installed on PCM-3102/3202 models.

D.1.6 CNX-II Board

For these descriptions, refer to Figure 7-14 on page 7-18 of this manual. The configuration of JU-1, JU-2, JU-3, and JU-4 are at the operators discretion. The APR-5003V Series (which incorporate the use of this board) machines have the capability of either an analog differential line output or an RS-422 output for the LTC port. The normal factory configuration is JU-1 and JU-3 installed. If a change to the output stage of the LTC signal is desired, follow the guidelines shown in the jumper descriptions that follow. JU-5 and JU-6 have been retired for this board revision.

- JU-1** : Normally IN on the APR-5000 Series, this jumper (used in conjunction with JU-3) connects the High side of the DLO (Differential Line Output) hybrid (IC14) to the LTC OUT connector on the rear panel. If this jumper is used, JU-3 MUST be installed.
- JU-2** : Normally OUT on the APR-5000 Series, this jumper (used in conjunction with JU-4) connects the High side of the RS-422 output driver (IC16A pin 2), a 26LS31, to the LTC OUT connector on the rear panel. If this jumper is used, JU-4 MUST be installed.
- JU-3** : Normally IN on the APR-5000 Series, this jumper (used in conjunction with JU-1) connects the Low side of the DLO (Differential Line Output) hybrid (IC14) to the LTC OUT connector on the rear panel. If this jumper is used, JU-1 MUST be installed.
- JU-4** : Normally OUT on the APR-5000 Series, this jumper (used in conjunction with JU-2) connects the Low side of the RS-422 output driver (IC16A, pin 3), a 26LS31, to the LTC OUT connector on the rear panel. If this jumper is used, JU-2 MUST be installed.
- JU-5** : This jumper has been retired.
- JU-6** : This jumper has been retired.
- JU-7** : Normally OUT on the APR-5000 Series, this jumper (used in the PCM-3102/3202 machines only) connects the ground to capacitors C5 and C6. This enables the function of the low pass filter configuration of R18, R19, C5 and C6 (Fc=100kHz). This jumper is ONLY installed on PCM-3102/3202 models.
- JU-8** : Normally OUT on the APR-5003V Series, this jumper is used to bypass the VVT board LTC/VITC port selector. With this jumper installed, ONLY the LTC port data will be input to the CPU as EXT TC RX.

D.1.7 CPU Board

For these descriptions, refer to Figure 7-16A on page 7-20 of this manual. The most recent revision of the CPU board retired many of the jumpers that were originally mounted on this board. Jumpers JW-1, JW-2, and JW-5 through JW-11 have been retired. The remaining two jumpers (JW-3 and JW-4) are described below.

JW-3 : Normally IN on the APR-5000 Series, this jumper is installed when the RAM chips to be used are 8K X 8-bit Read/Write memory ICs. JW-3 and JW-4 are mutually exclusive.

JW-4 : Normally OUT on the APR-5000 Series, this jumper is installed when the RAM chips to be used are 2K X 8-bit Read/Write memory ICs. JW-3 and JW-4 are mutually exclusive.

D.1.8 CTM Board

There are no jumpers or switches located on this board.

D.1.9 DSP Board

There are no jumpers or switches located on this board.

D.1.10 FEX Board

There are no jumpers or switches located on this board.

D.1.11 HES Board

There are no jumpers or switches located on this board.

D.1.12 KBD Board

There are no jumpers or switches located on this board.

D.1.13 MSB Board

There are no jumpers or switches located on this board.

D.1.14 LNT Board

For these descriptions, refer to Figure 7-26 on page 7-32 of this manual. As described in Section 4 of this manual, the LNT board is a separate microprocessor (8085 type) system. This dedicated processor system is used specifically for serial control interfacing. The LNT board incorporates the use of four jumper blocks and one eight position DIP switch. These items are described below.

- JW-1** : Normally IN on the APR-5000 Series machines, this jumper serves no purpose to the system. This jumper is used on the PCM-3102/3202 machines ONLY to connect the CAP REF signal to the CTL board. The jumper is installed on the APR series for manufacturing purposes only.
- JW-2** : Normally OUT on the APR-5000 Series machines, this jumper is installed when a 256K ROM chip is used (standard configuration of present APR machines uses a 128K ROM, with software revision P1.01.01.03).
- JW-3** : Normally IN on the APR-5000 Series machines, this jumper is installed when a 2K X 8K SRAM (Static Random Access Memory) chip is used. JW-3 and JW-4 are mutually exclusive.
- JW-4** : Normally OUT on the APR-5000 Series machines, this jumper is installed when an 8K X 8K SRAM (Static Random Access Memory) chip is used. JW-3 and JW-4 are mutually exclusive.
- SW-1** : The switch position status for this switch is shown in Appendix E (Baud Rate Selection) of this manual.

D.1.15 MST Board (early model)

There are no jumpers or switches located on this board.

D.1.16 MST Board (late model)

For these descriptions, refer to Figure 7-30 on page 7-36 of this manual.

- JW-1** : Normally OUT on the APR-5000 Series machines.
- JW-2** : Normally IN on the APR-5000 Series machines.
- JW-3** : Normally OUT on the APR-5000 Series machines.
- JW-4** : Normally IN on the APR-5000 Series machines.

JW-5 : Normally OUT on the APR-5000 Series machines.

JW-6 : Normally IN on the APR-5000 Series machines, this jumper connects the output of the BIAS PULSE buffer (IC13A, pin 3) to the edge connector pin 24A. If this jumper is not installed, there will be no BIAS PULSE B (buffered bias pulse) signal fed to the CNL/TCC cards.

D.1.17 RMD Board

There are no jumpers or switches located on this board.

D.1.18 RTS (RTS-1) Board

There are no jumpers or switches located on this board.

D.1.19 SBR Board

There are no jumpers or switches located on this board.

D.1.20 TCC Board

For these descriptions, refer to Figure 7-35A and 7-35B on pages 7-42 and 7-43 of this manual.

JW-1 : Normally OUT on the APR-5000 Series, this jumper serves no real purpose in the TCC card since there is not a Reproduce head used.

JW-2 : Normally IN on the APR-5000 Series, this jumper connects the BIAS signal output (pin 8 of K2) to the edge connector pin 5A.

JW-3 : Normally IN on the APR-5000 Series, this jumper connects the ERASE signal output (pin 3 of K2) to the edge connector pin 6A.

JW-4 : This jumper has been retired.

JW-5 : This jumper has been retired.

D.1.21 TCM Board

There are no jumpers or switches located on this board.

D.1.22 TIB Board

For these descriptions, refer to Figure 7-37A and 7-37B on pages 7-45 and 7-46 of this manual.

JU-1 : Normally IN on the APR-5000 Series. When this jumper is removed, a test program is entered on the CPU board. Refer to Section 6.5.8.2 of this manual for the Variable Speed Adjustment Procedure.

JU-2 : Normally IN on the APR-5000 Series. This jumper is not utilized in present software. JU-2 should always be installed for proper machine performance.

D.1.23 TTS Board

There are no jumpers or switches located on this board.

D.1.24 VVT Board

For these descriptions, refer to Figure 7-39 on page 7-48 of this manual.

JU-1 : Normally IN on the APR-5003V Series, this jumper is installed when a video signal is to be input from the video port (BNC connector) on the rear panel. This is the configuration shipped from the factory.

JU-2 : Normally OUT on the APR-5003V Series, this jumper is installed when a sinewave or squarewave pilot tone signal is to be input from the video port (BNC connector) on the rear panel.

D.1.25 CSL Board

For these descriptions, refer to Figure 7-41 on page 7-50 of this manual. It should be noted that the CSL board (used in the APR-5000 machines) and the PCS board (used in the PCM-3102/3202 machines) have identical artwork. When referring to the schematic diagram, the components labeled with a double asterisk (**) are installed on the PCS assembly ONLY.

JW-1 : Normally OUT on the APR-5000 Series, this jumper is installed on the PCM-3102/3202 Series machines.

JW-2 : Normally IN on the APR-5000 Series, this jumper is required to connect the output of the phase comparator circuit to the input of the capstan motor driver circuit.

D.1.26 PDB Board

For these descriptions, refer to Figure 7-43 on page 7-52 and Figure 2-1 on page 2-2 of this manual.

S1 : The setting of this switch is crucial to the performance of the APR-5000 unit. Refer to Figure 2-1 page 2-2 of this manual.

S2 : The setting of this switch is crucial to the performance of the APR-5000 unit. Refer to Figure 2-1 page 2-2 of this manual.

D.1.27 Power Supply Regulator Boards (RGA, RGB, RGC, RGD, RG1, RG2)

There are no jumpers or switches located on this board.

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APPENDIX E
LNT BOARD
BAUD RATE SELECTION

For **APR-5003V** operations with all SONY Editor equipments, the baud rate is fixed at 38.4 kilobauds (kbaud). However, the **APR-5003V** may be used at slower baud rates to accomodate other applications. Such other applications could be software created by either the user or by independent developers, this software most likely being run on personal computers. Documentation on the **APR-5003V** serial control facilities will be made at a future date for use by independent developers.

Three baud rates are selectable via the DIP switch S1 on the LNT board, the switch functions being specified as follows:

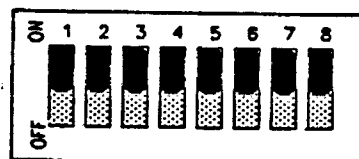
S1-1	Baud Rate Selection
S1-2	Baud Rate Selection
S1-3	Disable Video/Tone referenced operation*
S1-4	Not Assigned
S1-5	Not Assigned
S1-6	Not Assigned
S1-7	Not Assigned
S1-8	Reserved

* The facility provided by S1-3 is for use with those **APR-5003** models manufactured before the introduction of the **APR-5003V** which have been upgraded to accept **APR-5003V** software. This upgrade does not offer video or tone facilities, all synchronous operations being in reference to external Longitudinal Time Code.

DIP Switch Settings

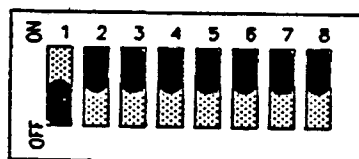
1. Normal Operation at 38.4 kbaud

S1-1	ON	S1-5	ON
S1-2	ON	S1-6	ON
S1-3	ON	S1-7	ON
S1-4	ON	S1-8	ON



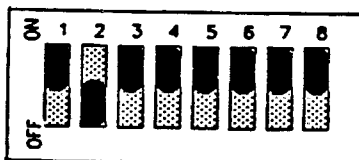
2. Special Operation at 19.2 kbaud

S1-1	OFF	S1-5	ON
S1-2	ON	S1-6	ON
S1-3	ON	S1-7	ON
S1-4	ON	S1-8	ON



3. Special Operation at 9.6 kbaud

S1-1	ON	S1-5	ON
S1-2	OFF	S1-6	ON
S1-3	ON	S1-7	ON
S1-4	ON	S1-8	ON



1. The first part of the document is a list of names and addresses. The names are listed in the first column, and the addresses are listed in the second column. The list is organized in a table format.

2. The second part of the document is a list of names and addresses. The names are listed in the first column, and the addresses are listed in the second column. The list is organized in a table format.

Name	Address
John Doe	123 Main St, New York, NY
Jane Smith	456 Elm St, Los Angeles, CA
Bob Johnson	789 Oak St, Chicago, IL
Alice Brown	101 Pine St, San Francisco, CA
Charlie White	202 Cedar St, Boston, MA
Diana Green	303 Birch St, Philadelphia, PA
Frank Black	404 Spruce St, Washington, DC
Grace King	505 Willow St, Miami, FL
Henry Lee	606 Ash St, Seattle, WA
Ivy Hill	707 Poplar St, Denver, CO
Jack Adams	808 Hickory St, Portland, OR
Karen Baker	909 Sycamore St, San Diego, CA
Liam Clark	1010 Magnolia St, Austin, TX
Mia Evans	1111 Dogwood St, Nashville, TN
Noah Foster	1212 Redwood St, San Jose, CA
Olivia Garcia	1313 Cypress St, Houston, TX
Peter Hall	1414 Juniper St, Salt Lake City, UT
Quinn Harris	1515 Fir St, Minneapolis, MN
Rachel King	1616 Hemlock St, Kansas City, MO
Samuel Lee	1717 Spruce St, Omaha, NE
Tina Miller	1818 Cedar St, Las Vegas, NV
Uma Patel	1919 Birch St, Phoenix, AZ
Victor Quinn	2020 Willow St, San Antonio, TX
Wendy Reed	2121 Ash St, Fort Worth, TX
Xavier Scott	2222 Spruce St, Dallas, TX
Yara Torres	2323 Cedar St, San Jose, CA
Zoe Vance	2424 Birch St, San Francisco, CA

3. The third part of the document is a list of names and addresses. The names are listed in the first column, and the addresses are listed in the second column. The list is organized in a table format.

4. The fourth part of the document is a list of names and addresses. The names are listed in the first column, and the addresses are listed in the second column. The list is organized in a table format.

5. The fifth part of the document is a list of names and addresses. The names are listed in the first column, and the addresses are listed in the second column. The list is organized in a table format.

6. The sixth part of the document is a list of names and addresses. The names are listed in the first column, and the addresses are listed in the second column. The list is organized in a table format.

Name	Address
John Doe	123 Main St, New York, NY
Jane Smith	456 Elm St, Los Angeles, CA
Bob Johnson	789 Oak St, Chicago, IL
Alice Brown	101 Pine St, San Francisco, CA
Charlie White	202 Cedar St, Boston, MA
Diana Green	303 Birch St, Philadelphia, PA
Frank Black	404 Spruce St, Washington, DC
Grace King	505 Willow St, Miami, FL
Henry Lee	606 Ash St, Seattle, WA
Ivy Hill	707 Poplar St, Denver, CO
Jack Adams	808 Hickory St, Portland, OR
Karen Baker	909 Sycamore St, San Diego, CA
Liam Clark	1010 Magnolia St, Austin, TX
Mia Evans	1111 Dogwood St, Nashville, TN
Noah Foster	1212 Redwood St, San Jose, CA
Olivia Garcia	1313 Cypress St, Houston, TX
Peter Hall	1414 Juniper St, Salt Lake City, UT
Quinn Harris	1515 Fir St, Minneapolis, MN
Rachel King	1616 Hemlock St, Kansas City, MO
Samuel Lee	1717 Spruce St, Omaha, NE
Tina Miller	1818 Cedar St, Las Vegas, NV
Uma Patel	1919 Birch St, Phoenix, AZ
Victor Quinn	2020 Willow St, San Antonio, TX
Wendy Reed	2121 Ash St, Fort Worth, TX
Xavier Scott	2222 Spruce St, Dallas, TX
Yara Torres	2323 Cedar St, San Jose, CA
Zoe Vance	2424 Birch St, San Francisco, CA

7. The seventh part of the document is a list of names and addresses. The names are listed in the first column, and the addresses are listed in the second column. The list is organized in a table format.

APPENDIX F
TAPE PATH
MECHANICAL ADJUSTMENTS

F.6 Overview

This appendix is provided to assist the service engineer with the tape path and mechanical head adjustment of the APR-5000 Series Recorders. The information contained herein can also be found in the APR-5000 Operation and Maintenance manual. Original section numbers remain for reference purposes.

F.1 APR-5000 Tape Path Mechanical Adjustments

6.5.6 Head Height

In order for the APR-5000 system to function properly the tape must remain in firm physical contact with the head surface at all times. Even the smallest misalignment may cause errors in level and response that may be incorrectly attributed to the electronics system. The tape must be evenly distributed across the entire head surface when passing across it in PLAY or RECORD mode. If the distribution is not even and the pressure is greater at one edge, this can result in skewing of the tape away from the center of the head. The head height adjustment is checked when the tape is not centered on the head surface.

Observe the tape movement across the heads. The tape should be centered between the two grooves which are machined into the surface of the head when checking the repro or sync head (see Figure 6-10). When adjusting the erase head make sure that the distance © is equal to the distance © in Figure 6-11. If adjustments are necessary refer to this procedure.

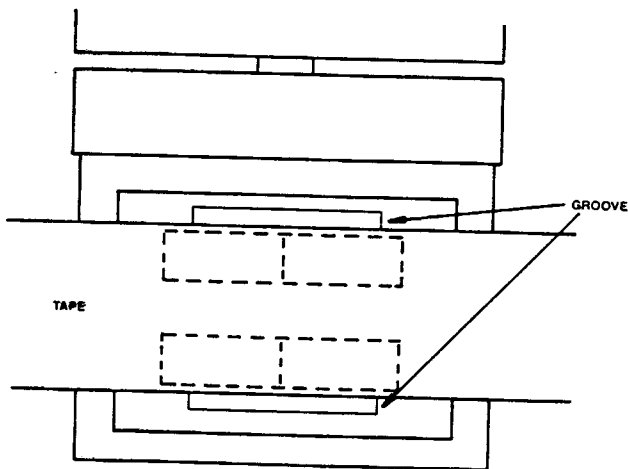


Figure: 6-10. Repro or Sync Head Heights

STEP 1 Turn the height adjustment screw (refer to Figure 6-12) clockwise to raise the head or counter clockwise to lower the head.

NOTE: This adjusts the height of the front of the head only.

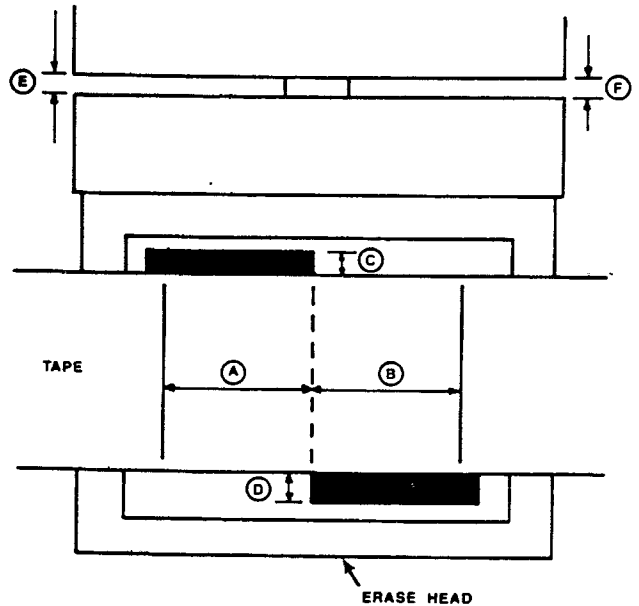


Figure 6-11. Erase Head Adjustments

STEP 2 Turn the zenith adjustment screw the in the same direction to compensate for the tilt created when adjusting the head height. This will adjust the height of the rear of the head. Visually inspect the head tilt with respect to the fast guides.

STEP 3 Turn the azimuth adjustment the same number of turns in the opposite direction to compensate for the tilt created by changing the height.

STEP 4 Always check the head zenith after adjusting the head height. (Refer to Section 6.5.7 Head Zenith Adjustment.)

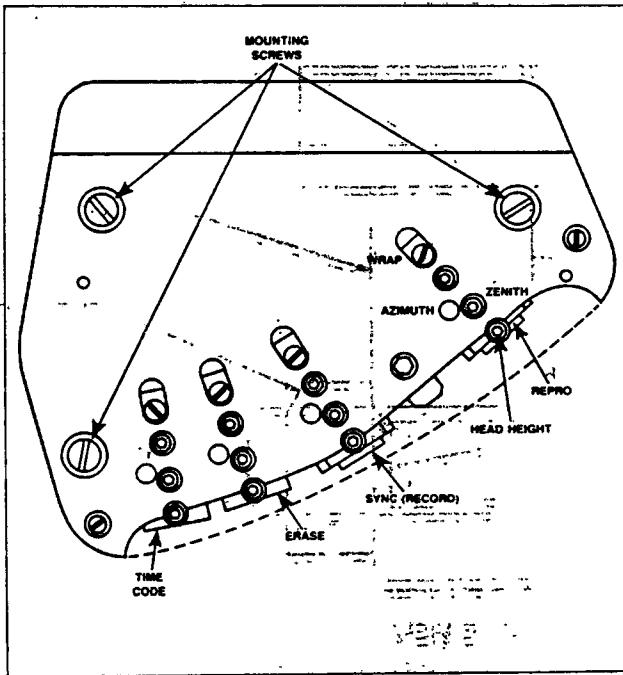


Figure 6-12. Headstack Adjustment Screws

6.5.7 Head Zenith Adjustment

The head zenith is always checked after the head height is adjusted or whenever tape path adjustments have been made. The head zenith is adjusted so that the head surface is parallel to the fixed guides. This adjustment will affect the overall tape path. The head zenith adjustment is made using the zenith block.

STEP 1 Turn the power OFF. Remove the headstack cover if installed then loosen the three headstack mounting screws using a driver. Remove the headstack from the machine by pulling upward.

STEP 2 Check that the DIP switch setting on the headstack. Assure that it is valid. (See Figure 6-13, Headstack Identification Codes.)

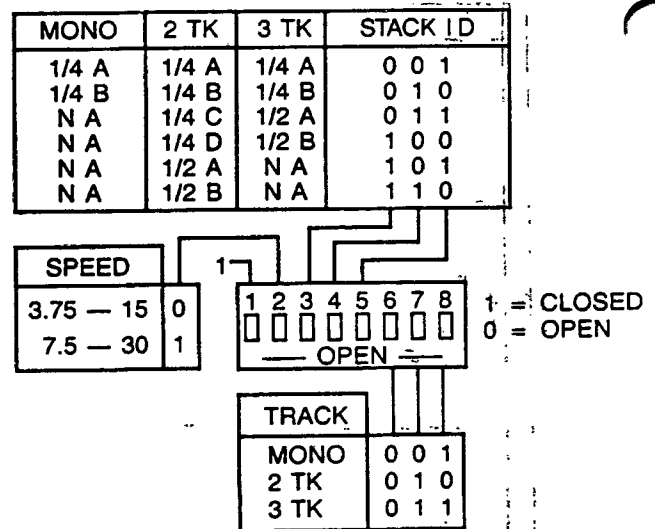


Figure 6-13. Headstack Identification Code

STEP 3 Visually inspect the heads by holding the headstack up to a source of light and applying the zenith block between the left tape guide and the erase head. Hold the block firmly on the tape guide and pivot the block so that it is lightly touching the erase head. Looking through the tape guide, the zenith error of the erase head will become visible. If no light is visible between the block and the erase head then the erase head is properly referenced to the left hand tape guide. (See Figure 6-14.)

STEP 4 Hold the headstack up to the light viewing from the left hand guide. Position the headstack so that the surface of the erase head is sighted to the surface of the record head. Shade the erase head with hand and observe any non-parallelism between the erase and record head surfaces. Adjust the record head zenith screw until both head surfaces are parallel.

STEP 5 Sight the sync head surface to the repro head surface using the same method in STEP 4. Adjust the repro head zenith adjustment until both head surfaces are parallel. Re-check by sighting from right tape guide.

STEP 6 Install the headstack on the deck. Use cau-

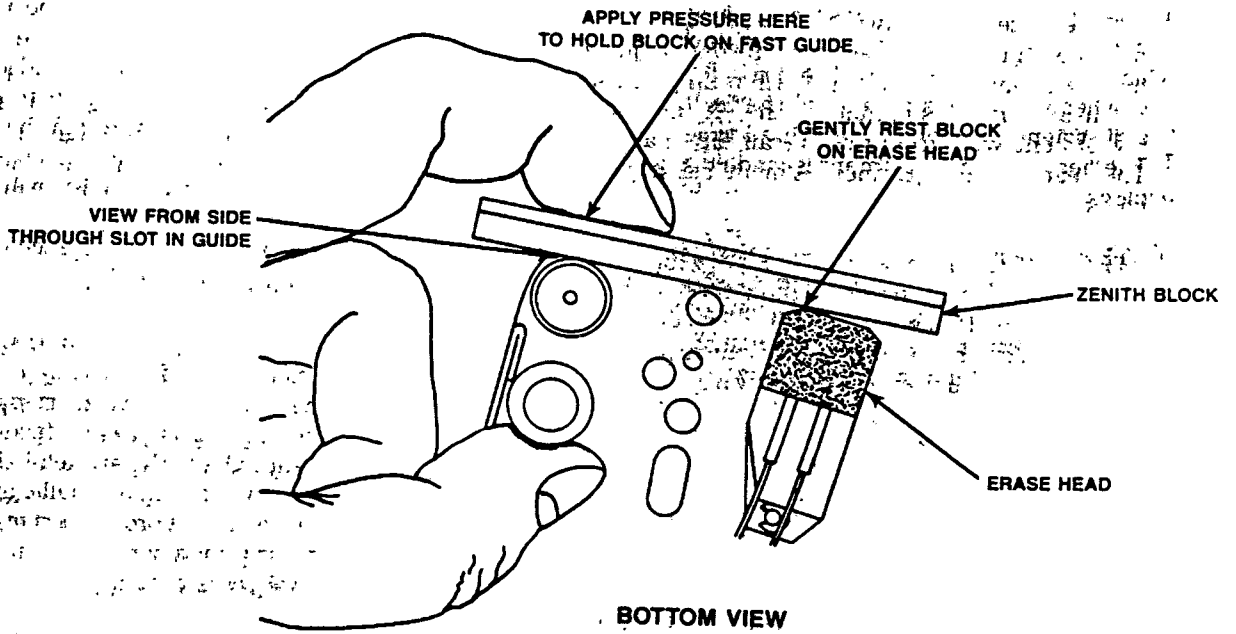
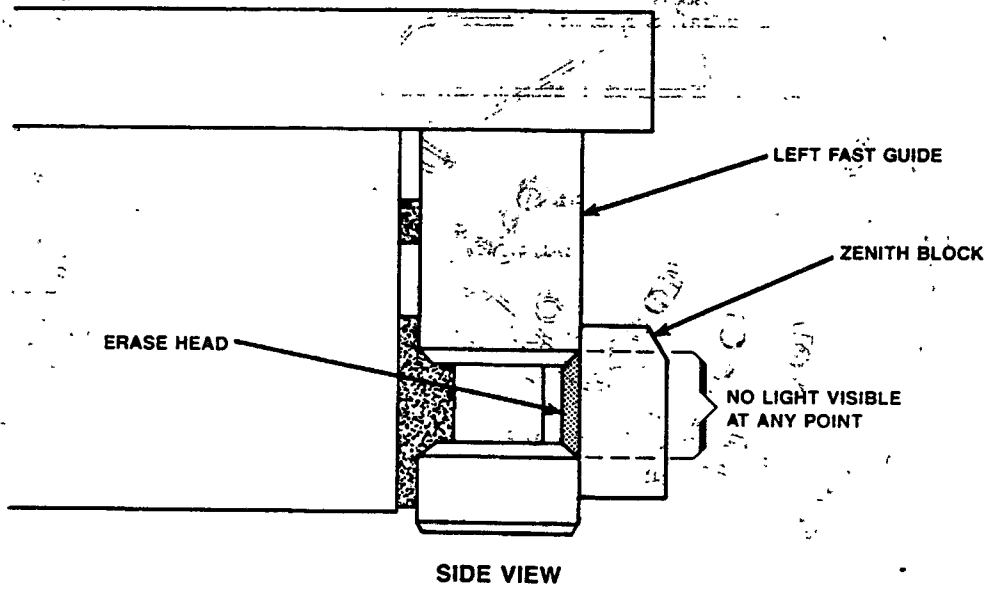


Figure 6-14. Erase Head Zenith

STEP 5 Move the flutter dampening arm to the left until it is in contact with its left stop. Check that a minimum reading of -5VDC is obtained.

STEP 6 Position the HES Board so that the absolute value of voltages obtained at each limit STOP are equal within $\pm 0.5\text{VDC}$.

STEP 7 Probe TPB on the board with the voltmeter.

STEP 8 Move the flutter dampening arm through its entire range. Adjust RV1 on the HES board so that the voltmeter reading changes 10.25 volts $\pm 0.25\text{VDC}$.

STEP 9 Move the flutter dampening arm so that it is in contact with its right side stop. Adjust RV2 on the HES board so that the voltmeter reads $0\text{VDC} \pm 0.25\text{V}$. Check that voltmeter reading at left limit stop is $+10.25\text{V}$, $\pm 0.25\text{V}$. Repeat STEPS 8 and 9 if required to meet specifications.

STEP 10 Thread a work tape onto the reels.

STEP 11 Loosen the screws labelled (A) and (B) in Figure 6-22.

STEP 12 Press **PLAY**. Adjust the spring assembly by plate (secured by screws (A)) so that the flutter dampening arm assembly is parallel with the edge of the HES assembly and there is an equal distance between the assembly and either of the stops. Tighten screws (A).

STEP 13 Adjust screw (B) to make sure that the bottom of the flutter dampening arm assembly has clearance from the spring (see Figure 6-23).

STEP 14 Press **STOP**.

6.5.13 Roller Guide Adjustments

The roller guides will rarely need to be adjusted unless there is repair to any of the mechanical parts

or for some reason, the original adjustment of these parts is disturbed. Check the tape path over each of the roller guides referring to Figure 6-24. If the tape is riding smoothly through each of the guides without wrinkling, pinching or noise in FAST FORWARD or REWIND mode, then adjustment is not necessary.

These adjustments are made using the roller guide height adjustment tool.

STEP 1 Remove front top cosmetic cover. (See Section 6.4.2.)

STEP 2 Turn the power ON and thread a work tape onto the reels (refer to Section 5 if unfamiliar with mounting of reels or threading of tape).

STEP 3 Place the machine in FAST FORWARD mode until almost all the tape is on the take-up reel.

STEP 4 Press **REW** and touch the MVC knob to enter the SPOOL WIND mode.

STEP 5 Observe the tape path over the timer roller. The tape should ride in the center of the guide, and no scraping, noise should be detectable. Make sure that the tape rides smoothly over the guide by visual inspection (refer to Figure 6-24 Tape Path).

STEP 6 If the tape is riding smoothly over the timer roller, skip STEPS 6 through 12.

STEP 7 Press **STOP** and unscrew the guide cap.

STEP 8 Attach the roller guide alignment tool (TS-2991-007-02) to the top of the roller guide shaft (be sure to use the correct side for the timer roller) and loosen the adjusting collar set screw with an 2.6mm hex Allen driver.

STEP 9 Press **REW** and then touch the MVC knob (SPOOL WIND).

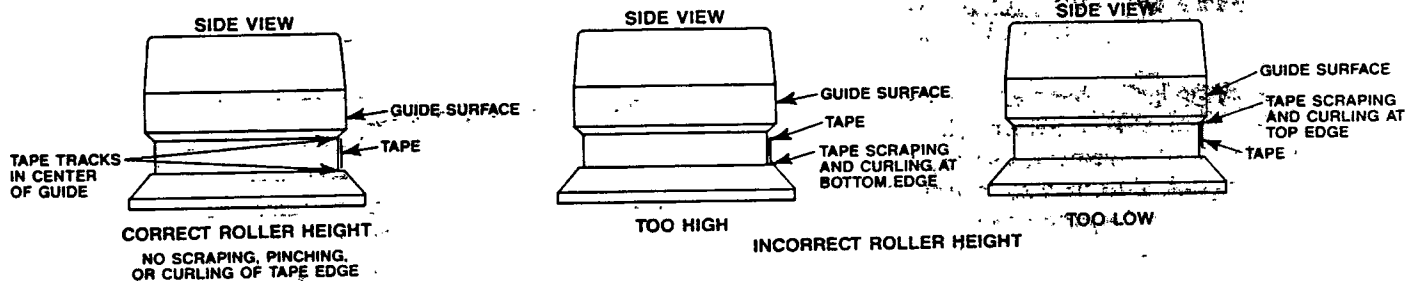


Figure 6-24. Tape Path Over the Roller Guides

STEP 10 Observe the tape path over the roller guide and turn the guide alignment tool clockwise or counter-clockwise until the tape rides in the center of the roller guide and no scraping noise is detectable. Visually inspect that the tape rides smoothly over the roller guide (refer to Figure 6-24 Tape Path).

STEP 11 Tighten the collar adjusting set screw.

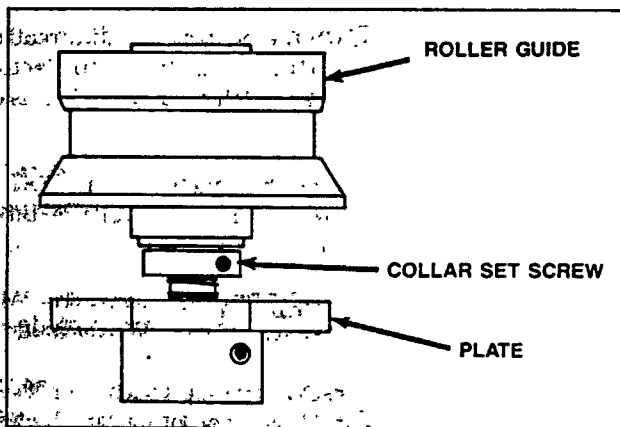


Figure 6-25. Roller Guide Height Adjustment

STEP 12 Press **STOP** and remove the roller guide alignment tool. Replace the roller guide cap.

STEP 13 Press **REW** and then touch the MVC knob (SPOOL WIND).

STEP 14 Observe the tape path over the S-Roller. The tape should ride in the center of the guide and no scraping noise should be detectable. Make sure that the tape rides smoothly over the guide by visual inspection (refer to Figure 6-24, Tape Path).

STEP 15 If a height adjustment is required then repeat STEPS 6 through 11.

STEP 16 Press **FFWD** and touch the MVC knob (SPOOL WIND).

STEP 17 Observe the tape path over the S-guide and the timer roller. No scraping, curling, or pinching should be observed. Re-adjust the timer roller and the S-guide if the tape path is incorrect.

STEP 18 Press **PLAY** and observe the tape path over the T-guide. The tape should track the center of the T-guide (the same as the S-guide and the timer roller).

STEP 19 If a height adjustment is required then repeat STEPS 6 through 11 using the other side of the same roller guide alignment tool. (The earlier model TS-2991-007-01 c also be used here.)

STEP 20 Press **FFWD** and touch the MVC knob (SPOOL WIND).

STEP 21 Re-check the tape path over the T-guide and re-adjust if it is incorrect.

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